TRANSPORTATION ELECTRICAL EQUIPMENT SPECIFICATIONS

TEES

NOTE: The symbol (*) denotes that a word, number, phrase, sentence or specification has been changed, deleted or added to the previous TEES Document.

MARCH 29, 2002

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CHAPTER 1

GENERAL SPECIFICATIONS FOR ELECTRICAL EQUIPMENT

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CHAPTER 1 SECTION 1

GLOSSARY

1.1 Wherever the following terms or abbreviations are used, the intent and meaning shall be interpreted as follows:

A	**-**	**Ampere**
AASHTO	**-**	**American Association of State Highway and Transportation Officials**
AC	**-**	**Alternating Current**
AC+	**-**	**120 Volts AC, 60 hertz ungrounded power source**
AC-	**-**	**120 Volts AC, 60 hertz grounded return to the power source**
AGENCY	**-**	**Purchasing Government Agency**
ANSI	**-**	**American National Standard Institute**
API	**-**	**Application Program Interface**
ASCII	**-**	**American Standard Code for Information Interchange**
Assembly	**-**	**A complete machine, structure or unit of a machine that was manufactured by fitting together parts and/or modules**
ASTM	**-**	**American Society for Testing and Materials**
ATC	**-**	**Advanced Transportation Controller**
AWG	**-**	**American Wire Gage**
bps	**-**	**bits per second**
C	**-**	**Celsius**
C Language	**-**	**The ANSI C Programming Language**
Cabinet	**-**	**An outdoor enclosure generally housing the controller unit and associated equipment**

Certificate of Compliance	**-**	**A certificate signed by the manufacturer of the material or the manufacturer of assembled materials stating that the materials involved comply in all respects with the requirements of the specifications**
Channel	**-**	**An information path from a discrete input to a discrete output**
CIA	**-**	**CMS Controller Isolation Assembly**
CIP	**-**	**CMS Interface Panel**
CMOS	**-**	**Complementary Metal Oxide Semiconductor**
CMS	**-**	**Changeable Message Sign**
CMS SYSTEM	**-**	**Includes Controller Unit, Model 334C Cabinet, Interconnect Harnesses, CMS and other associated equipment required to operate the system.**
Component	**-**	**Any electrical or electronic device**
Contractor	**-**	**The person or persons, manufacturer, firm, partnership, corporation, vendor or combination thereof, who have entered into a contract with the AGENCY, as party(s) of the second part or legal representative**
Controller Unit	**-**	**That portion of the controller assembly devoted to the operational control of the logic decisions programmed into the assembly**
CPDA	**-**	**CMS Pixel Driver Assembly**
CPDM	**-**	**CMS Pixel Driver Module**
CPMM	**-**	**CMS Pixel Matrix Module**
CPU	**-**	**Central Processing Unit**
CR	**-**	**ACIA Control Register**
CRC	**-**	**Cyclic Redundancy Check**
DAT Program	**-**	**The AGENCYs Diagnostic and Acceptance Test Program**
Daughter Board	**-**	**(from TechEncyclopedia) A Printed Circuit Board that plugs into another Printed Circuit Board to augment its capabilities**
dB	**-**	**Decibel**

dBa	**-**	**Decibels above reference noise, adjusted**
DC	**-**	**Direct Current**
DIN	**-**	**Deutsche Industrie Norm**
DMA	**-**	**Direct Memory Access**
DMS	**-**	**Dynamic Message Sign**
DTA	**-**	**Down Time Accumulator**
DTE	**-**	**Data Terminal Equipment**
DTR	**-**	**Data Terminal Ready**
EG	**-**	**Equipment Ground**
EIA	**-**	**Electronic Industries Association**
EMI	**-**	**Electro Magnetic Interference**
Engineer	**-**	**The AGENCY director, acting either directly or through properly authorized agents, such agents acting within the scope of the particular duties delegated to them**
EPROM	**-**	**Ultraviolet Erasable, Programmable, Read Only Memory Device**
EEPROM	**-**	**Electrically Erasable, Programmable, Read Only Memory Device**
Equal	**-**	**Connectors: comply to physical dimensions, contact material, plating and method of connection. Devices: conforming to function, pin out, electrical and operating parameter requirements, access times and interface parameters of the specified device**
ETL	**-**	**Electrical Testing Laboratories, Inc.**
FCU	**-**	**Field Controller Unit.**
Firmware	**-**	**A computer program or software stored permanently in PROM, EPROM, ROM or semi-permanently in EEPROM**
FLASH	**-**	**A +5 VDC powered IC Memory Device with nonvolatile, electrically erasable, programmable, 100K read/write minimum cycles and fast access time features**

FPA	**-**	**Front Panel Assembly**
HDLC	**-**	**High-Level Data Link Control**
HEX	**-**	**Hexadecimal**
Hz	**-**	**Hertz**
IC	**-**	**Integrated Circuit**
I.D.	**-**	**Identification**
IEEE	**-**	**Institute of Electrical and Electronics Engineers**
IP	**-**	**Internet Protocol**
IPI	**-**	**Initial Protocol Identifier**
ISP	**-**	**Information Service Provider**
ISO	**-**	**International Standards Organization**
ITE	**-**	**Institute of Transportation Engineers**
ITS	**-**	**Intelligent Transportation Systems**
Jumper	**-**	**A means of connecting/disconnecting two or more conductive by soldering/desoldering a conductive wire or by PCB post jumper**
KB	**-**	**Kilobytes**
Laboratory	**-**	**The established laboratory of the AGENCY or other laboratories authorized by the AGENCY to test materials involved in the contract**
LED	**-**	**Light Emitting Diode**
LOGIC	**-**	**Negative Logic Convention (Ground True) State**
LSB	**-**	**Least Significant Byte**
lsb	**-**	**Least Significant Bit**
MB	**-**	**MegaByte**
MSB	**-**	**Most Significant Byte**

msb	**-**	**Most Significant Bit**
m	**-**	**Milli**
MCU/MPU/ IMP	**-**	**Micro Controller Unit, Microprocessor Unit, or Integrated Multiprotocol Processor**
MIL	**-**	**Military Specifications**
MODEM	**-**	**Modulation/Demodulation Unit**
Module	**-**	**A functional unit that plugs into an assembly**
Motherboard	**-**	**A printed circuit connector interface board with no active or passive components**
MOS	**-**	**Metal-Oxide Semiconductor**
MOV	**-**	**Metal-Oxide Varistor**
MS	**-**	**Military Standards**
M/170	**-**	**Program Module/Model 170 Controller Unit Connector**
M/170E	**-**	**Model 170E Auxiliary Board Connector**
N	**-**	**Newton: SI unit of force**
N.C.	**-**	**Normally closed contact**
N.O.	**-**	**Normally open contact**
NA	**-**	**Presently Not Assigned. Cannot be used by the contractor for other purposes**
NEMA	**-**	**National Electrical Manufacturer's Association**
NETA	**-**	**National Electrical Testing Association, Inc.**
n	**-**	**nano**
NLSB	**-**	**Next Least Significant Byte**
nlsb	**-**	**Next Least Significant Bit**
NMSB	**-**	**Next Most Significant Byte**

nmsb	**-**	**Next Most Significant Bit**
NTCIP	**-**	**National Transportation Communication for ITS Protocol**
PCB	**-**	**Printed Circuit Board**
PDA	**-**	**Power Distribution Assembly**
PLA/PAL	**-**	**Programmable Array Logic Device**
Power Failure	**-**	**A Power Failure is said to have occurred when the incoming line voltage falls below 92 +/- 2 VAC for 50 ms. See Power Conditions.**
Power Restoration	**-**	**Power is said to be restored when the incoming line voltage equals or exceeds 97 +/- 2 VAC for 50 ms. See Power Conditions.**
Power Conditions	**-**	**16.7 ms (one 60 Hz cycle) reaction period is allowed to be included in the 50 ms timing or added to (67 ms duration). The hysteresis between power failure and power restoration voltage settings shall be a min. of 5 VAC with a threshold drift of no more than 0.2 VAC**
PMPP	**-**	**Point-to-Multi-Point Protocol**
ppm	**-**	**Parts per million**
PPP	**-**	**Point-to-Point Protocol**
PWM	**-**	**Pulse Width Modulation**
RAM	**-**	**Random Access Memory**
RDR	**-**	**ACIA Receiver Data Register**
RF	**-**	**Radio Frequency**
RMS	**-**	**Root-Mean-Square**
ROM	**-**	**Read Only Memory Device**
RTC	**-**	**Model 170E Controller Unit Real Time Clock. This circuitry provides a 170E CPU IRQ Interrupt pulse clocked off of the local power company's line frequency every 16.67 ms.**
RTCA	**-**	**Real Time Clock Adjuster Circuitry**

RTS	**-**	**Request to Send**
R/W	**-**	**Model 170E Controller Unit Read/Write Control Line**
SCI	**-**	**Serial Communications Interface**
SDLC	**-**	**Synchronous Data Link Control**
S	**-**	**Logic State**
s	**-**	**second**
Second Sourced	**-**	**Produced by more than one manufacturer**
SR	**-**	**ACIA Status Register**
SRAM	**-**	**Static Random Access Memory Device**
SW	**-**	**Switch**
TB	**-**	**Terminal Block**
TDR	**-**	**ACIA Transmit Data Register**
TIA	**-**	**Telecommunications Industry Association**
TOD	**-**	**Time Of Day Clock**
Triac	**-**	**Silicon-Controlled Rectifier which controls power bilaterally in an AC switching circuit**
TTL	**-**	**Transistor-Transistor Logic**
Thumb Screw Device	**-**	**(TSD) A retractable screw fastener with projecting stainless steel screw, spring and natural aluminum knob finish. (TSD No. 2 shall be flat black.)** **TSD No.1 - 8-32 SOUTHCO #47-62-301-20 or equal.** **TSD No.2 - 8-32 SOUTHCO #47-62-301-60 or equal.** **TSD No.3 - M3 SOUTHCO #47-82-101-10 or equal.**
µ	**-**	**Micro**
UL	**-**	**Underwriter's Laboratories, Inc.**

VAC	**-**	**Voltage Alternating Current**
VDC	**-**	**Voltage Direct Current**
VMA	**-**	**Valid Memory Address**
VME	**-**	**Versa Module Eurocard, VMEbus Standard IEEE P1014/D1.2**
VMS	**-**	**Variable Message Sign**
x	**-**	**Number Value**
XX	**-**	**Manufacturer's Option**
WDT	**-**	**Watchdog Timer: A monitoring circuit, external to the device watched, which senses an Output Line from the device and reacts**

CHAPTER 1 SECTION 2

GENERAL

1.2.1
In CASE of CONFLICT, the individual chapter shall govern over Chapter 1.

1.2.2
All furnished equipment shall be new and unused. Vacuum or gaseous tubes and electro-mechanical devices (unless specifically called out) shall not be used.

1.2.3
INTERCHANGEABILITY - The following assemblies and their respective associated devices shall electrically and mechanically intermate and be compatible with each other:

ASSEMBLIES	ASSOCIATED DEVICES
Output File #1 & #2	- Model 200 Switch Pack - Model 210 Monitor Unit - Model 430 Heavy Duty Relay
Input File	- Models 222, 224, & 232E Detectors - Models 242 & 252 Isolators
PDA #2	- Model 204 Flasher Unit - Model 206 Power Supply Module
PDA #3	- Model 200 Switch Pack - Model 206 Power Supply Module - Model 208 Monitor Unit - Model 430 Heavy Duty Relay
PDA #4	- Model 206 Power Supply - CMS Isolation Module
Model 170E Controller Unit	- Cabinet Models 332, 334 & 336 - Model 400 MODEM - Model 412C Program Module
Model 2070 Controller Unit	- Cabinet Models 332, 334, 336 & ITS - Model 2070-1 CPU Module - Model 2070-2 Field I/O Module - Model 2070-3 Front Panel Assembly - Model 2070-4 Power Supply - Model 2070-5 VME Cage Assembly - Model 2070-6 Serial Comm Module

	- Model 2070-7 Serial Comm Module
Input Assembly	- Model 222, 222E, 232E & 224 Sensor Unit - Model 242 and 252 Isolator Unit - Model 218 Serial Interface Unit (SIU)
Output Assembly	- Model 200 Switch Pack Unit - Model 205 FTR Relay - Model 214 Auxiliary Monitor Unit - Model 218 SIU Unit
PDA ITS	- 2 Model 204 Flasher Units - Model 212 Cabinet Monitor Unit - Model 216-12 & 216-24 Power Supply Units
Model 2070-N1 Controller Unit	- Model 2070 Controller Unit - Model 2070-8 NEMA Module - Model 2070-4N Field I/O Module
Model 2070-N2 Controller Unit	- Model 2070-2N Field I/O Module - Model 2070-4N Power Supply Module
Pixel Driver Assembly	- Pixel Driver Module

1.2.4 DOCUMENTATION

1.2.4.1
Two copies of Manual Documentation shall be supplied for each item purchased up to 200 manuals per order. The manual shall be bound in durable covers made of either 65-pound stock paper or clear plastic. The manual shall be printed on 215.9 mm by 279.4 mm paper, with the exception that schematics, layouts, parts lists and plan details may be on 279.4 mm by 431.8 mm sheets, with each sheet neatly folded to 215.9 mm by 279.4 mm size. Manual text font shall be HELVETICA BOLD. Text characters shall be no more than 10 characters per 25.4 mm and 7 lines per 25.4 mm, with the exception of schematic text, which shall be no more than 18 characters per 25.4 mm and 11 lines per 25.4 mm.

1.2.4.2
Each manual shall include the following parts in the order listed:

1. **Table of Contents**
2. **Glossary**
3. **General Description**
4. **General Characteristics**
5. **Installation**
6. **Adjustments**

7. **Theory of Operation**
    a. **Systems Description (include block diagram).**
    b. **Detailed Description of Circuit Operation.**
8. **Maintenance**
    a. **Preventive Maintenance.**
    b. **Trouble Analysis.**
    c. **Trouble Shooting Sequence Chart.**
    d. **Wave Forms.**
    e. **Voltage Measurements.**
    f. **Alignment Procedures.**
9. **Parts List (include circuit and board designation, part type and class, power rating, component manufacturer, mechanical part manufacturer, data specification sheets for special design components and original manufacturer's part number).**
10. **Electrical Interconnection Details & Drawings.**
11. **Schematic and Logic Diagram.**
12. **Assembly Drawings and a pictorial diagram showing physical locations and identification of each component or part.**
13. **The date, serial numbers and revision numbers of equipment covered by the manuals shall be printed on the front cover of the manuals.**

1.2.4.3
Manuals for the cabinet shall be furnished in the cabinet plastic pouch.

1.2.4.4
A preliminary draft of the manual shall be submitted to the Engineer for approval prior to final printing.

1.2.5
PACKAGING - Each item delivered shall be individually packed in its own shipping container. When loose styrofoam is used for packing the item, the item shall be sealed in a plastic bag to prevent direct contact with the styrofoam.

1.2.6
DELIVERY - Each item delivered for testing shall be complete, including manuals, and ready for testing.

1.2.7 METALS

1.2.7.1
ALUMINUM - Sheet shall be 63 gage American Standard (0.062 inch) minimum thick Type 3003-H14 or Type 5052-H32 ASTM Designation B209 aluminum alloy. Rod, Bar and Extruded shall be Type 6061-T6, or equal.

1.2.7.2
STAINLESS STEEL - Sheet shall be annealed or one-quarter-hard complying with the ASTM Designation: A666 for Type 304, Grades A or B, stainless steel sheet.

1.2.7.3
COLD ROLLED STEEL - Sheet, Rod, Bar and Extruded shall be Type 1018/1020.

1.2.7.3.1
Plating - All cold roll steel shall be plated. All plating shall be either cadmium plating meeting the requirements of Federal Specification QQ-P-416C, Type 2 Class l or zinc plating meeting the requirements of ASTM B633-85 Type II SC4.

1.2.7.4
All sharp edges and corners shall be rounded.

1.2.8
All bolts, nuts, washers, screws (size 8 or larger), hinges and hinge pins shall be stainless steel unless otherwise specified.

1.2.9
Within the circuit of any device, module, or PCB, electrical isolation shall be provided between DC logic ground, equipment ground and the AC grounded conductor. They shall be electrically isolated from each other by 500 megohms, minimum, when tested at the input terminals with 100 VDC.

1.2.10
DAUGHTER BOARDS – Keyboards and LCD/LED Displays are considered daughter boards. Daughter boards shall be mechanically secured with a minimum of four spacers / metal screws. Connectors shall be either Flat Cable or PCB Headers. Components are allowed to be mounted under the daughter board.

CHAPTER 1 SECTION 3

COMPONENTS

1.3.1
GENERAL - All components shall be second sourced and shall be of such design, fabrication, nomenclature or other identification as to be purchased from a wholesale distributor or from the component manufacturer, except as follows:

1.3.1.1
When a component is of such special design that it precludes the purchase of identical components from any wholesale distributor or component manufacturer, one spare duplicate component shall be furnished with each 20, or fraction thereof, components used.

1.3.1.2
The electronic circuit design shall be such that all components of the same generic type, regardless of manufacturer, shall function equally in accordance with the specifications.

1.3.2 ELECTRONIC COMPONENTS

1.3.2.1
No device shall be socket mounted unless specifically called out or requested and approved at Qualified Product List Submittal.

1.3.2.2
No component shall be operated above 80% of its maximum rated voltage, current or power ratings. Digital components shall not be operated above 3% over their nominal voltage, current or power ratings.

1.3.2.3
No component shall be provided where the manufactured date is 3 years older than the contract award date. The design life of all components, operating for 24 hours a day and operating in their circuit application, shall be 10 years or longer.

1.3.2.4
Encapsulation of 2 or more discrete components into circuit modules is prohibited except for transient suppression circuits, resistor networks, diode arrays, solid-state switches, optical isolators and transistor arrays. Components shall be arranged so they are easily accessible, replaceable and identifiable for testing and maintenance. Where damage by shock or vibration exists, the component shall be supported mechanically by a clamp, fastener, retainer, or hold-down bracket.

1.3.2.5
The Contractor shall submit detailed engineering technical data on all components at the request of the Engineer. A letter from the component manufacturer shall be submitted with the detailed engineering data when the proposed application of the component alters the

technical data. The letter shall certify that the component application meets specification requirements.

1.3.3
CAPACITORS - The DC and AC voltage ratings as well as the dissipation factor of a capacitor shall exceed the worst-case design parameters of the circuitry by 150%. Capacitor encasements shall be resistant to cracking, peeling and discoloration. All capacitors shall be insulated and shall be marked with their capacitance values and working voltages. Electrolytic capacitors shall not be used for capacitance values of less than 1.0 microfarad and shall be marked with polarity.

1.3.4
POTENTIOMETERS - Potentiometers with ratings from 1 to 2 watts shall meet Military Type RV4 requirements. Under 1 Watt potentiometers shall be used only for trimmer type function. The potentiometer power rating shall be at least 100% greater than the maximum power requirements of the circuit.

1.3.5
RESISTORS - Fixed carbon film, deposited carbon, or composition-insulated resistors shall conform to the performance requirements of Military Specifications MIL-R-11F or MIL-R-22684. All resistors shall be insulated and shall be marked with their resistance values. Resistance values shall be indicated by the EIA color codes, or stamped value. The value of the resistors shall not vary by more than 5% between -37 ^{0}C and 74 ^{0}C.

1.3.5.1
Special ventilation or heat sinking shall be provided for all 2-watt or greater resistors. They shall be insulated from the PCB.

1.3.6 SEMICONDUCTOR DEVICES

1.3.6.1
All solid-state devices, except LED's, shall be of the silicon type.

1.3.6.2
All transistors, integrated circuits, and diodes shall be a standard type listed by EIA and clearly identifiable.

1.3.6.3
All metal oxide semiconductor components shall contain circuitry to protect their inputs and outputs against damage due to high static voltages or electrical fields.

1.3.6.4
Device pin "1" locations shall be properly marked on the PCB adjacent to the pin.

1.3.7
TRANSFORMERS AND INDUCTORS - All power transformers and inductors shall have the manufacturer's name or logo and part number clearly and legibly printed on the case

or lamination. All transformers and inductors shall have their windings insulated, shall be protected to exclude moisture, and their leads color coded with an approved EIA color code or identified in a manner to facilitate proper installation.

1.3.8
TRIACS - Each triac with a designed circuit load of greater than 0.5 Amperes at 120 VAC shall be mounted to a heat sink with a machine screw and nut with integral lockwasher.

1.3.9
CIRCUIT BREAKERs shall be listed by UL or ETL. The trip and frame sizes shall be plainly marked (marked on the breaker by the manufacturer), and the ampere rating shall be visible from the front of the breaker. Contacts shall be silver alloy and enclosed in an arc-quenching chamber. Overload tripping shall not be influenced by an ambient air temperature range of from -18 degrees C to 50 degrees C. The minimum Interrupting Capacity shall be 5,000 Amperes, RMS when the breaker is secondary to a UL approved fuse or primary circuit breaker and both breakers in concert provide the rated capacity. For circuit breakers 80 amperes and above, the minimum interrupting capacity shall be 10,000 amperes, RMS. Circuit breakers shall be the trip-free type with medium trip delay characteristic (Carling switch Time Delay Curve #24 or equal).

1.3.10
All FUSEs shall be 3AG Slow Blow type and resident in a holder. Fuse size rating shall be labeled on the holder. Fuses shall be easily accessible and removable without use of tools.

1.3.11 SWITCHES

1.3.11.1
DIP - Dual-inline-package, quick snap switches shall be rated for a minimum of 30,000 operations per position at 50 ma, 30 VDC. The switch contact resistance shall be 100 milliohms maximum at 2 ma, 30 VDC. The contacts shall be gold over brass (or silver). Contact for VAC or 28 VDC and shall be silver over brass (or equal).

1.3.11.2
LOGIC - The switch contacts shall be rated for a minimum of one ampere resistive load at 120 VAC and shall be silver over brass (or equal). The switch shall be rated for a minimum of 40,000 operations.

1.3.11.3
CONTROL - The switch contacts shall be rated for a minimum of five ampere resistive load at 120 VAC or 28 VDC and shall be gold over brass (or equal). The switch shall be rated for a minimum of 40,000 operations.

1.3.11.4
POWER - Ratings shall be the same as CONTROL, except the contact rating shall be a minimum of ten amperes at 125 VAC.

1.3.12
TERMINAL BLOCKS - The terminal blocks shall be barrier type, rated at 20 amperes and 600 VAC RMS minimum. The terminal screws shall be 7.938 mm minimum length nickel plated brass binder head type with screw inserts of the same material. Screw size is called out under the associated file, panel or assembly.

1.3.13 WIRING, CABLING AND HARNESSES

1.3.13.1
HARNESSES shall be neat, firm and properly bundled with external protection. They shall be tie-wrapped and routed to minimize crosstalk and electrical interference. Each harness shall be of adequate length to allow any conductor to be connected properly to its associated connector or termination point. Conductors within an encased harness have no color requirements.

1.3.13.2
Wiring containing AC shall be bundled separately or shielded separately from all DC logic voltage control circuits.

1.3.13.3
Wiring shall be routed to prevent conductors from being in contact with metal edges. Wiring shall be arranged so that any removable assembly may be removed without disturbing conductors not associated with that assembly.

1.3.13.4
All conductors shall conform to MIL-W-16878E/1 or better and shall have a minimum of 19 strands of copper. The insulation shall be polyvinyl chloride with a minimum thickness of 10 mils or greater. Where insulation thickness is 15 mils or less, the conductor shall conform to MIL-W-16878/17.

1.3.13.5
Conductor color identification shall be as follows:

Grounded AC circuits - gray or white
Equip. Ground - solid green or continuous green color with 1 or more yellow stripes.
DC logic ground - continuous white with a red stripe.
Ungrounded AC+ - continuous black or black with colored stripe.
DC logic ungrounded or signal - any color not specified

1.3.14
INDICATORS AND CHARACTER DISPLAYS - All indicators and character displays shall be readily visible at a radius of up to 1.2 m (4 feet) within the cone of visibility when the indicator is subjected to 97,000 lux (9,000 foot-candles) of white light with the light source at 45 +/-2 degrees to the front panel.

1.3.14.1
INDICATORS - All indicators and character displays shall have a minimum 90 degrees cone of visibility with its axis perpendicular to the panel on which the indicator is mounted. All indicators shall be self-luminous. All indicators shall have a rated life of 100,000 hours minimum. Each LED indicator shall be white or clear when off and invisible when on. Indicators supplied on equipment requiring handles shall be mounted such that a horizontal clearance of 15 degrees minimum shall be provided for Models 208, 210, 212, 222, 232, 242 and 252, as well as a clearance of 30 degrees minimum for Models 200, 204 and 206.

1.3.14.2
CHARACTER DISPLAYS - Liquid Crystal Displays (LCD) shall operate at temperatures of -20 ^{0}C to +70 ^{0}C.

1.3.15 CONNECTORS

1.3.15.1
GENERAL - All connectors shall be keyed to prevent improper insertion of the wrong connector. The mating connectors shall be designated as the connector number and male/female relationship, such as C1P (plug or PCB edge connector) and C1S (socket).

1.3.15.2
The TYPE T connector shall be a single row, 10 position, feed through terminal block. The terminal block shall be a barrier type with 6-32, 6.35 mm or longer, nickel plated brass binder head screws. Each terminal shall be permanently identified as to its function.

1.3.15.3
PLASTIC CIRCULAR and M TYPE CONNECTORS - Pin and socket contacts for connectors shall be beryllium copper construction subplated with 0.00127 mm nickel and plated with 0.00076 mm gold. Pin diameter shall be 1.57 mm. All pin and socket connectors shall use the AMP #601105-1 or #91002-1 contact insertion tool and the AMP #305183 contact extraction tool.

1.3.15.4
CARD EDGE and TWO-PIECE PCB CONNECTORS

1.3.15.4.1
PCB edge connectors shall have bifurcated gold-plated contacts. The PCB receptacle connector shall meet or exceed the following:

Operating Voltage:	**600 VAC (RMS)**
Current Rating:	**5.0 amperes**
Insulation Material:	**Diallyl Phthalate or Thermoplastic**
Insulation Resistance:	**5,000 megohms**

Contact Material:	**Copper alloy plated with 0.00127 mm (0.00005 inch) of nickel and 0.000381 mm (0.000015 inch) of gold**
Contact Resistance:	**0.006 ohm maximum**

1.3.15.4.2
The two-piece PCB connector shall meet or exceed the DIN 41612.

1.3.15.4.3
The PCB 22/44 Connector shall have 22 independent contacts per side; dual sided with 3.96 mm (0.156 inch) contact centers.

1.3.15.4.4
The PCB 28/56 Connector shall have 28 independent contacts per side, dual sided with 3.96 mm (0.156 inch) contact centers.

1.3.15.4.5
The PCB 36/72 Connector shall have 36 independent contacts per side, dual sided with 2.54 mm (0.100 inch) contact centers.

1.3.15.4.6
The PCB 43/86 Connector shall have 43 independent contacts per side, dual sided with 2.54 mm (0.100 inch) contact centers.

1.3.15.5
WIRE TERMINAL CONNECTORS - Each wire terminal shall be solderless with PVC insulation and a heavy duty short -locking spade type connector. All terminal connectors shall be crimped using a Controlled-Cycle type crimping tool.

1.3.15.6
FLAT CABLE CONNECTORS - Each flat cable connector shall be designed for use with 26 AWG cable; shall have dual cantilevered phosphor bronze contacts plated with 508 nm of gold over 1270 nm of nickel; and shall have a current rating of 1 A minimum and an insulation resistance of 5 megohms minimum.

1.3.15.7
PCB HEADER POST CONNECTORS - Each PCB header post shall be 1.0 mm square by 8.7 mm high; shall be mounted on 4.0 mm centers; and shall be tempered hard brass plated with 381 nm of gold over 1.270 mm of nickel.

1.3.15.8
PCB HEADER SOCKET CONNECTORS - Each PCB header socket block shall be nylon or diallyl phthalate. Each PCB header socket contact shall be removable, but crimp-connected to its conductor. The Contractor shall list the part number of the extraction tool recommended by its manufacturer. Each PCB header socket contact shall be brass or phosphor bronze plated with 562 nm of gold over 1270 nm of nickel.

1.3.16

SURGE PROTECTION DEVICE - A three-electrode gas tube type that is capable of withstanding 15 pulses of peak current each of which will rise in 8 us and fall in 20 us to 0.5 of the peak voltage at 3-minute intervals. Peak current rating shall be 20,000 amperes. It shall have the following ratings:

IMPULSE BREAKDOWN:	**Less than 1,000 volts in less than 0.1 us at 10 KV/us.**
STANDBY CURRENT:	**Less than 1 ma.**
STRIKING VOLTAGE:	**Greater than 212 volts.**

CHAPTER 1 SECTION 4

MECHANICAL

1.4.1
ASSEMBLIES - All assemblies shall be modular, easily replaceable and incorporate plug-in capability for their associated devices or PCBs. Assemblies shall be provided with 2 guides for each plug-in PCB or associated device (except relays). The guides shall extend to within 19.05 mm from the face of either the socket or connector and front edge of the assembly. If Nylon guides are used, the guides shall be securely attached to the file or assembly chassis.

1.4.2
PCB DESIGN - No components, traces, brackets or obstructions shall be within 3.175 mm of the board edge (guide edges). The manufacturer's name or logo, model number, serial number, and circuit issue or revision number shall appear and be readily visible on all PCBs. Devices to prevent PC Board from backing out of their assembly connectors shall be provided.

1.4.3
MODEL NUMBERS - The manufacturer's model number, serial number, and circuit issue or revision number shall appear on the rear panel of all equipment supplied (where such panel exists). In addition to any assignment of model numbers by the manufacturer, the State model number shall be displayed on the front panel in bold type, at least 6.35 mm high.

1.4.4
All PCB connectors mounted on a motherboard shall be mechanically secured to the chassis or frame of the unit or assembly.

1.4.5
All screw type fasteners shall utilize locking devices or locking compounds except for finger screws, which shall be captive.

1.4.6
WORKMANSHIP - Workmanship shall conform with the requirements of this specification and be in accordance with the highest industry standards.

1.4.7
TOLERANCES - The following tolerances shall apply, except as specifically shown on the plans or in these specifications:

Sheet Metal	**+/-**	**1.334 mm (0.0525 inch)**
PCB	**+/-**	**0.254 mm (0.010 inch)**
Edge Guides	**+/-**	**0.381 mm (0.015 inch)**

CHAPTER 1 SECTION 5

ENGINEERING

1.5.1 HUMAN ENGINEERING

1.5.1.1
The equipment shall be engineered for simplicity, ease of operation and maintenance.

1.5.1.2
Knobs shall be a minimum of 12.7 mm in diameter and a minimum separation of 12.7 mm edge to edge.

1.5.1.3
PCBs shall slide smoothly in their guides while being inserted into or removed from the frame and shall fit snugly into the plug-in PCB connectors. PCBs shall require a force no less than 22.24 N or greater than 222.4 N for insertion or removal.

1.5.2
DESIGN ENGINEERING - The design shall be inherently temperature compensated to prevent abnormal operation. The circuit design shall include such compensation as is necessary to overcome adverse effects due to temperature in the specified environmental range. Personnel shall be protected from all dangerous voltages.

1.5.3
GENERATED NOISE - No item, component or subassembly shall emit a noise level exceeding the peak level of 55 dBa when measured at a distance of one meter away from its surface, except as otherwise noted. No item, component or subassembly shall emit a noise level sufficient to interfere with processing and communication functions of the controller circuits.

CHAPTER 1 SECTION 6

PRINTED CIRCUIT BOARDS

1.6.1 DESIGN, FABRICATION AND MOUNTING

1.6.1.1
All contacts on PCBs shall be plated with a minimum thickness of 0.000763 mm gold over a minimum thickness of 0.001905 mm nickel.

1.6.1.2
PCB design shall be such that when a component is removed and replaced, no damage is done to the board, other components, conductive traces or tracks.

1.6.1.3
Fabrication of PCBs shall be in compliance with Military Specification MIL-P-13949, except as follows:

1.6.1.3.1
NEMA FR-4 glass cloth base epoxy resin copper clad laminates 1.590 mm minimum thickness shall be used. Inter-component wiring shall be by laminated copper clad track having a minimum weight of 0.556 kilogram per square meter with adequate cross section for current to be carried. All copper tracks shall be plated or soldered to provide complete coverage of all exposed copper tracks. Jumper wires to external PCB components shall be from plated-through padded holes and as short as possible.

1.6.1.3.2
In Section 3.3 of Military Specification MIL-P-13949G Grade of Pits and Dents shall be of Grade B quality (3.5.1.3) or better. Class of permissible bow or twist shall be Class C (Table V) or better. Class of permissible warp or twist shall be Class A (Table II) or better.

1.6.1.3.3
Sections 4.2 through 6.6 of Military Specification MIL-P-13949G (inclusive) shall be omitted except as referenced in previous sections of this specification.

1.6.1.4
The mounting of parts and assemblies on the PCB shall conform to Military Specification MIL-STD-275E, except as follows:

1.6.1.4.1
Semiconductor devices that dissipate more than 250 mW or cause a temperature rise of 10 degrees C or more shall be mounted with spacers, transipads or heat sinks to prevent contact with the PCB.

1.6.1.4.2
When completed, all residual flux shall be removed from the PCB.

1.6.1.4.3
The resistance between any 2 isolated, independent conductor paths shall be at least 100 megohms when a 500 VDC potential is applied.

1.6.1.4.4
All PCBs shall be coated with a moisture resistant coating.

1.6.1.4.5
Where less than 6.35 mm lateral separation is provided between the PCB (or the components of a PCB) and any metal surface, a 0.79375 +/-0.39624 mm thick Mylar (polyester) plastic cover shall be provided on the metal to protect the PCB.

1.6.1.5
Each PCB connector edge shall be chamfered at 30 degrees from board side planes. The key slots shall also be chamfered so that the connector keys are not extracted upon removal of board or jammed upon insertion. The key slots shall be 1.143 +/- 0.127 mm for 2.54 mm spacing and 1.40 +/- 0.127 mm for 3.96 mm spacing.

1.6.2 SOLDERING

1.6.2.1
Hand soldering shall comply with Military Specification MIL-STD-2000.

1.6.2.2
Automatic flow soldering shall be a constant speed conveyor system with the conveyor speed set at optimum to minimize solder peaks or points. Temperature shall be controlled to within +/- 8 degrees C of the optimum temperature. The soldering process shall result in the complete coverage of all copper runs, joints and terminals with solder except that which is covered by an electroplating process. Wherever clinching is not used, a method of holding the components in the proper position for the flow process shall be provided.

1.6.2.2.3
If exposure to the temperature bath is of such time-temperature duration, as to come within 80% of any component's maximum specified time-temperature exposure, that component shall be hand soldered to the PCB after the flow process has been completed.

1.6.3
DEFINITIONS - Definitions for the purpose of this section on PCBs shall be taken from MIL-P-55110D Section 3.3 and any current addendum.

1.6.4
JUMPERS Jumpers are not allowed unless called out in the specifications or approved upon submittal at Qualified Products List Time.

CHAPTER 1 SECTION 7

QUALITY CONTROL

1.7.1
COMPONENTS - All components shall be lot sampled to assure a consistent high conformance standard to the design specification of the equipment.

1.7.2
SUBASSEMBLY, UNIT OR MODULE - Complete electrical, environmental and timing compliance testing shall be performed on each module, unit, printed circuit or subassembly. Housing, chassis, and connection terminals shall be inspected for mechanical sturdiness, and harnessing to sockets shall be electrically tested for proper wiring sequence. The equipment shall be visually and physically inspected to assure proper placement, mounting, and compatibility of subassemblies.

1.7.3
PREDELIVERY REPAIR

1.7.3.1
Any defects or deficiencies found by the inspection system involving mechanical structure or wiring shall be returned through the manufacturing process or special repair process for correction.

1.7.3.2
PCB flow soldering is allowed a second time if copper runs and joints are not satisfactorily coated on the first run. Under no circumstances shall a PCB be flow soldered more than twice.

1.7.3.3
Hand soldering is allowed for printed circuit repair.

CHAPTER 1 SECTION 8

ELECTRICAL, ENVIRONMENTAL AND TESTING REQUIREMENTS

1.8.1
GENERAL - The requirements called out in these specification dealing with equipment evaluation are a minimum guide and shall not limit the testing and inspection to insure compliance.

1.8.2
CERTIFICATION - These test procedures shall be followed by the Contractor who shall certify that they have conducted inspection and testing in accordance with these specifications.

1.8.3
INSPECTION - A visual and physical inspection shall include mechanical, dimensional and assembly conformance of all parts of these specifications.

1.8.4
ENVIRONMENTAL & ELECTRICAL - All components shall properly operate within the following limits unless otherwise noted:

Applied Line Voltage: 90 to 135 VAC, note "Power Failure / Restoration" limits
Frequency: 60 (+/-3.0) Hertz
Humidity: 5% to 95%
Ambient Temperature: -37 ^{0}C to +74 ^{0}C
Shock - Test per Specification MIL-STD-810E Method 516.4.
Vibration - per Specification MIL-STD-810E Method 514.4, equipment class G.

1.8.4.1
All circuits, unless otherwise noted, shall commence operation at or below 90 VAC as the applied voltage is raised from 50 to 90 VAC at a rate of 2 (+/-0.5) volts / second.

1.8.4.2
All equipment shall be unaffected by transient voltages normally experienced on commercial power lines. Where applicable, equipment purchased separately from the cabinet (which normally is resident) will be tested for compliance in a State accepted cabinet connected to the commercial power lines.

1.8.4.3
The power line surge protection shall enable the equipment being tested to withstand (nondestructive) and operate normally following the discharge of a 25 microfarad capacitor, charged to plus and minus 2,000 volts, applied directly across the incoming AC line at a rate of once every 10 seconds for a maximum of 50 occurrences per test. The unit under test will be operated at 20 ^{0}C (+/-5) ^{0}C and at 120 (+/-12) VAC.

1.8.4.4
The equipment shall withstand (nondestructive) and operate normally when one discharge pulse of plus or minus 300 volts is synchronously added to its incoming AC power line and moved uniformly over the full wave across 360 degrees or stay at any point of Line Cycle once every second. Peak noise power shall be 5 kilowatts with a pulse rise time of 500 ns. The unit under test will be operated at 20 ^{0}C (+/-5) ^{0}C and at 120 (+/-12) VAC.

1.8.4.5
The controller unit communications modules shall be tested resident in a State-accepted controller unit which in turn is housed in the cabinet.

1.8.4.6
CMS system equipment will be tested for compliance as a complete system with power from commercial power lines applied at the CMS CIP Panel and the CMS Power Surge Protector deactivated or removed.

1.8.4.7
Equipment shall comply only with the requirements of UL Bulletin of Research No. 23, "Rain Tests of Electrical Equipment."

1.8.4.8
All equipment shall continue normal operation when subjected to the following:

1.8.4.8.1
Low Temperature Test - With the item functioning at a line voltage over Electrical Range of Device in its intended operation, the ambient temperature shall be lowered from 20 ^{0}C to –37 ^{0}C at a rate of not more than 18 ^{0}C per hour. The item shall be cycled at -37 ^{0}C for a minimum of 5 hours and then returned to 20 ^{0}C at the same rate. The test shall be repeated with the line voltage at 135 VAC.

1.8.4.8.2
High Temperature Test - With the item functioning at a line voltage of 90 VAC in its intended operation, the ambient temperature shall be raised from 20 ^{0}C to 70 ^{0}C at a rate of not more than 18 ^{0}C per hour. The item shall be cycled at 70 ^{0}C for 5 hours and then returned to 20 ^{0}C at the same rate. The test shall be repeated with the line voltage at 135 VAC.

1.8.4.8.3
All equipment shall resume normal operation following a period of at least 5 hours at -37 ^{0}C and less than 10 percent humidity and at least 5 hours at 70 ^{0}C and 22% humidity, when 90 VAC is applied to the incoming AC.

1.8.4.9
The relative humidity and ambient temperature values in the following table shall not be exceeded.

AMBIENT TEMPERATURE VERSUS RELATIVE HUMIDITY AT BAROMETRIC PRESSURES (29.92 In. Hg.)

Ambient Temperature/ Dry Bulb (in ^{0}C)	Relative Humidity (in percent)	Ambient Temperature/ Wet Bulb (in ^{0}C)
-37.0 to 1.1	10	-17.2 to 42.7
1.1 to 46.0	95	42.7
48.8	70	42.7
54.4	50	42.7
60.0	38	42.7
65.4	28	42.7
71.2	21	42.7
74.0	18	42.7

1.8.4.10
All equipment shall be capable of normal operation following opening and closing of contacts in series with the applied voltage at a rate of 30 openings and closings per minute for a period of 2 minutes in duration.

1.8.5 CONTRACTOR'S TESTING CERTIFICATION

1.8.5.1
A complete QC / final test report shall be supplied with each item. The test report shall indicate the name of the tester and shall be signed by a responsible manager.

1.8.5.2
The quality control procedure and test report format shall be sullied to the Engineer for approval within 15 days following the award of the contract. The quality control procedure shall include the following:

Acceptance testing of all supplied components.
Physical and functional testing of all modules and items.
A minimum 100-hour burn-in of all equipment.
Physical and functional testing of all items.

CHAPTER 1 SECTION 9

CHAPTER DETAILS

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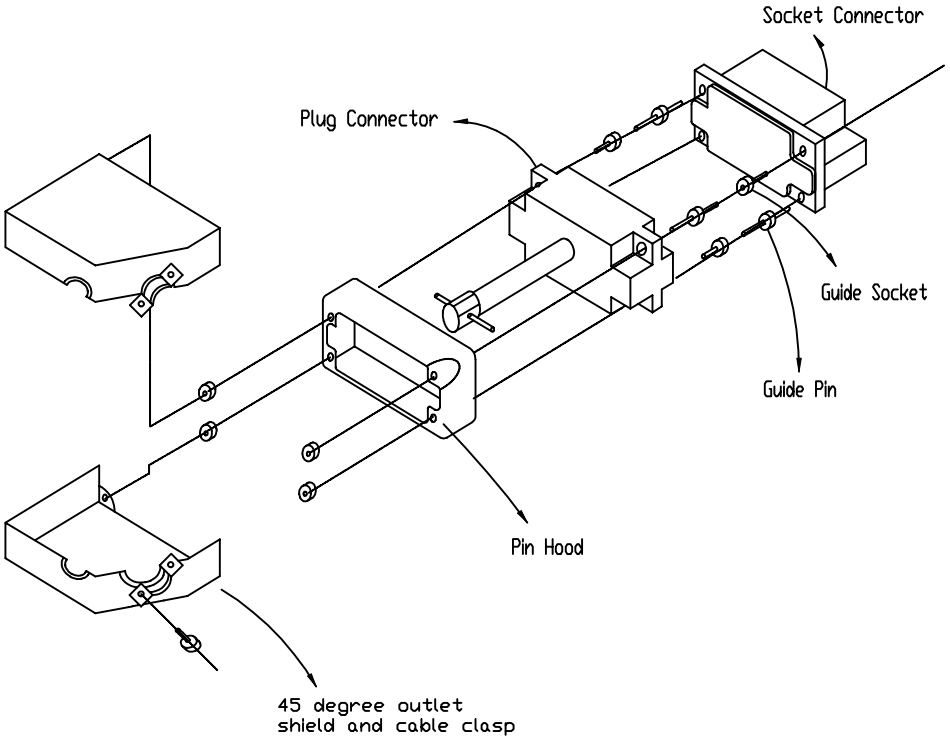
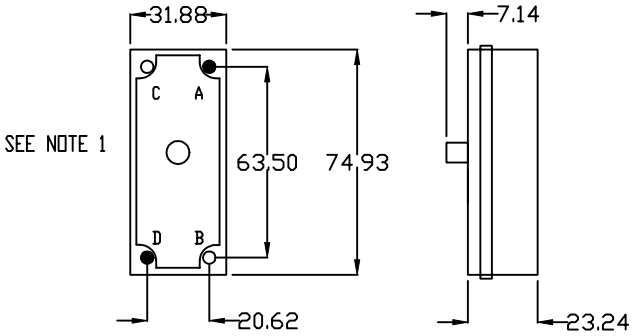
Section Notes:

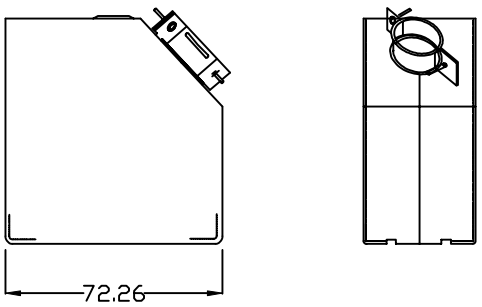
1. **All dimensions are in millimeters.**
2. **M Type connector blocks shall be constructed of phenolic or equal and shall have an insulation resistance of 5000 megohms. The contacts shall be secured in the blocks with stainless steel springs.**
3. **M Type connector corner guides shall be stainless steel. The guide pins shall be 27.86 in length and the guide sockets shall be 15.66 in length.**
4. **Circular plastic connectors shall have quick connect / disconnect capability and thread assist positive detent coupling. The connectors shall be UL listed glass-filled nylon, 94 V-I rated, heat stabilized and fire resistant.**



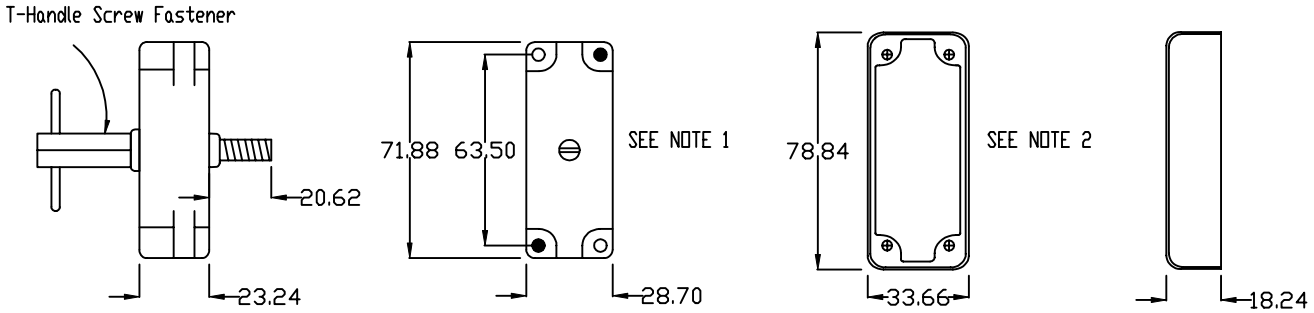
M104 CONNECTOR C1 DETAIL



M104 SOCKET CONNECTOR



M104 SHIELD



CONNECTOR C1P

M104 HOOD

NOTES:

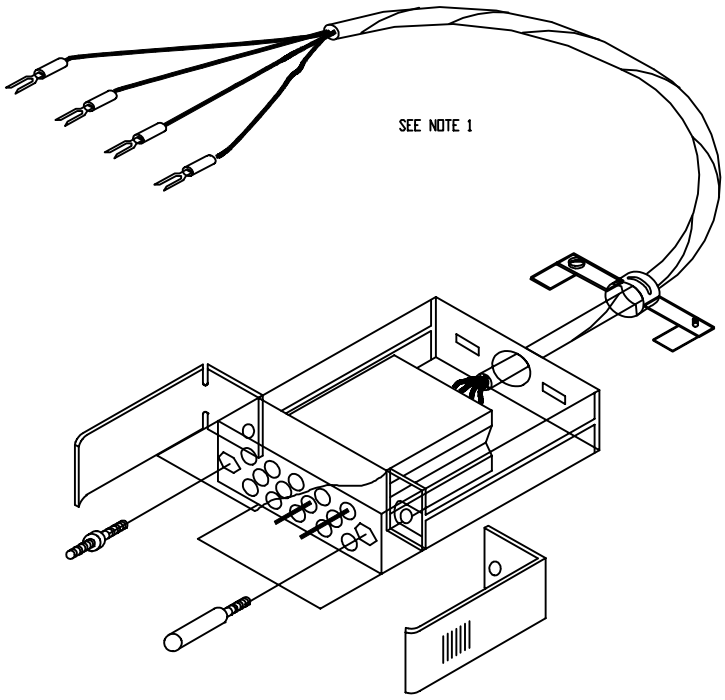
1. The darker circles denote guide pin location and the open circles are guide sockets.

2. Provide clearance for M104 plug with hood when mounting to it's socket.

TITLE:

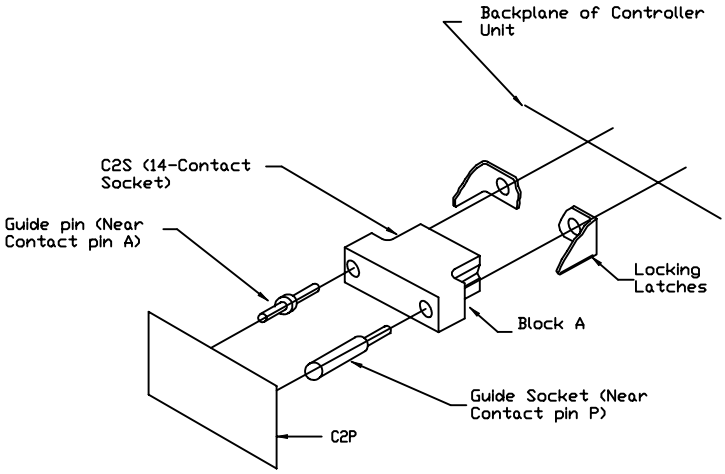
CONNECTOR DETAIL - M104

	NO SCALE	
	MARCH 29, 2002	1-9-1

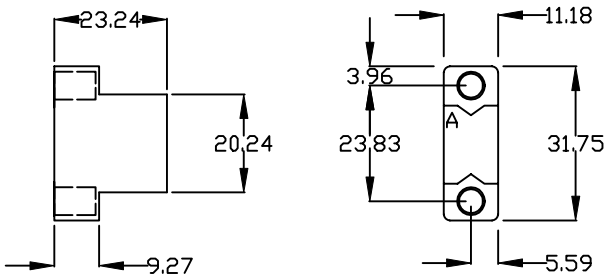


C2P MODEM INTERCONNECT HARNESS

C2P CONNECTOR ASSIGNMENT		
PIN	FUNCTION	WIRE COLOR
A	AUDIO IN	WHITE
B	AUDIO IN	GREEN
C	AUDIO OUT	RED
E	AUDIO OUT	BLACK



CONNECTOR C2 DETAIL

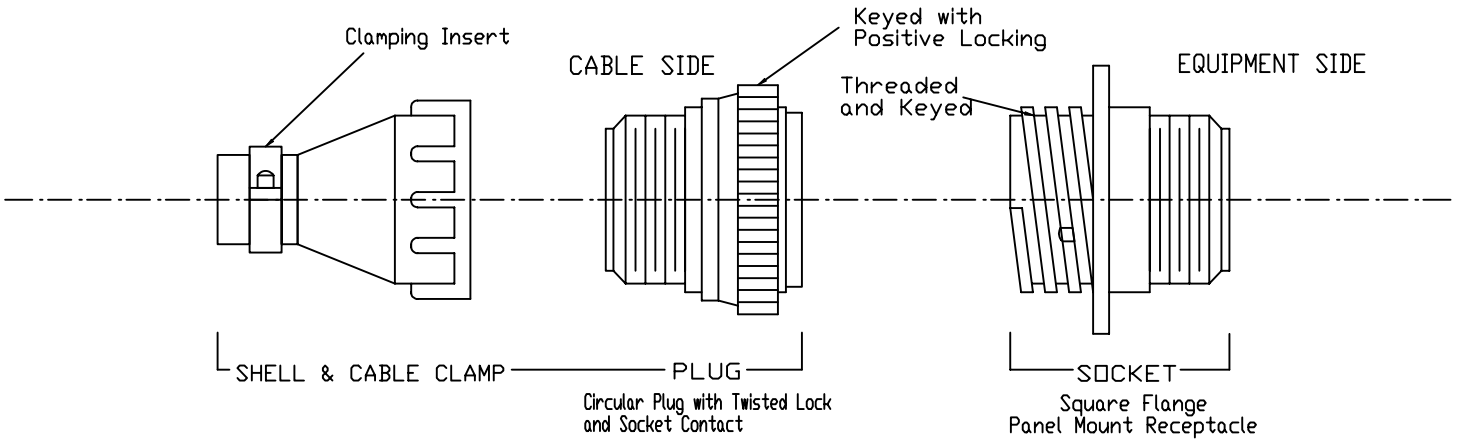


CONNECTOR C2S

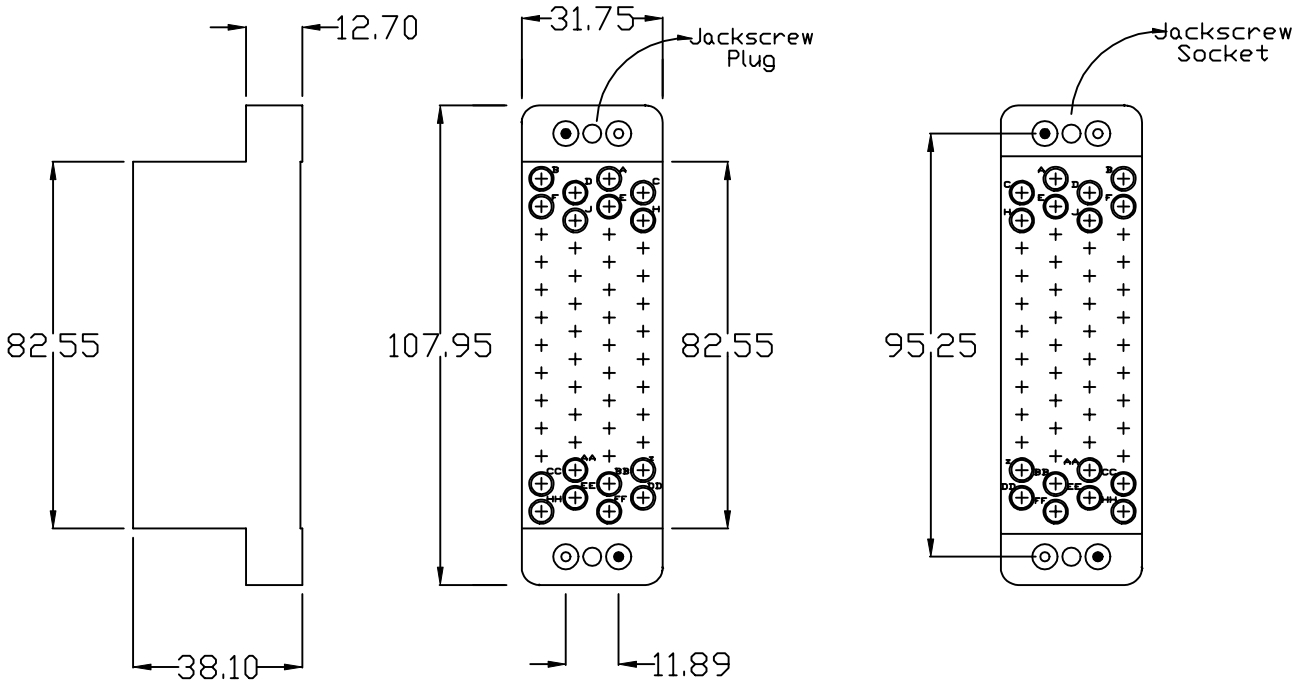
NOTES:

1. Cable length shall be 914 mm minimum. The cable shall be 2-pair #20 cable conductors, Belden 9402 or equal. The field end connections shall be #8 stud spring spade type.

TITLE: CONNECTOR DETAIL - M14	
NO SCALE	
MARCH 29, 2002	1-9-2



PLASTIC CIRCULAR PLUG AND SOCKET CONNECTOR



CONNECTOR PIN ARRANGEMENT

NOTES:

1. Guide Pins & Sockets, and Jackscrews are centered symmetrical to connector.

2. Key: o - socket
   ● - plug

TITLE: CONNECTOR DETAIL M50 & CIRCULAR PLASTIC CONNECTORS		
	NO SCALE	
	MARCH 29, 2002	1-9-3

CHAPTER 2

SPECIFICATIONS FOR MODEL 170E ENHANCED CONTROLLER UNIT AND ASSOCIATED MODULES

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CHAPTER 2 SECTION 1

GENERAL

2.1.1
System READ Access Time - With Model 412C Module Resident in the Controller Unit, valid data shall be present at the MPU at least 100 ns prior to the end of the machine cycle.

2.1.2
DIAGNOSTIC AND ACCEPTANCE TEST (DAT) PROGRAMS - The DAT-170E Program shall be provided resident on the Model 412C Program Module U1 memory device and on the CPU U6 memory device. A copy of the DAT Programs will be available to the contractor at no charge.

2.1.3
If a PAL, EPROM, or ROM device is used in address decoding and timing algorithms, the device code listing together with data sheet(s) and any specific coding requirements shall be included in the unit or module documentation. The device coding shall be delivered in the same form that the Contractor uses to directly reproduce the device.

2.1.4
SYSTEM ADDRESS ORGANIZATION - The system address organization of the Model 170E shall consist of two addressing configurations. The Decoder Input shall be furnished jumpered in address configuration 1. The internal module address organization shall be as specified in the appropriate module section.

2.1.4.1
The two addressing configurations shall be selectable by use of one post jumper. The jumper shall control the Logic State of one Decoder Circuit Input. The logic line shall be a three-post type with the two logic levels on the outer posts. The following input line state conditions shall cause the Decoder circuit to provide the associated address configurations:

CONFIGURATION	LINE	FUNCTION
1	+5 VDC	170E / 412C
2	DC GND	170E INTERNAL / 170

2.1.4.2
CONFIGURATION 1 Address Organization

FUNCTION	ADDRESS RANGE	COMMENTS
CPU SRAM	0000 - 0FFF	
U4 Memory	1000 - 3FFF	412C

Reserved	**4000**	**-**	**4FFF**
DTA Minutes	**5000**		**READ**
DTA Reset	**5000**		**WRITE**
INPUT / OUTPUT	**5001**	**-**	**5008**
	5009	**-**	**500A WRITE**
RESTART State	**5004**		**BIT 1 READ**
DTA Seconds	**500F**		**READ**
Reserve	**5009**	**-**	**500E READ**
	500B	**-**	**500F WRITE**
	5010	**-**	**5FFE**

CPU STATUS	**5FFF**	**READ**	**Bit 1 - ACIA #1 IRQ** **Bit 2 - ACIA #2 IRQ** **Bit 3 - ACIA #3 IRQ** **Bit 4 - ACIA #4 IRQ** **Bit 5 - Reserved** **Bit 6 – Address Configuration** **Bit 7 - DTA Timeout** **Bit 8 - RTC IRQ**

RTC Reset	**5FFF**		**WRITE**
ACIA #1	**6000**		**WRITE CR, READ SR**
ACIA #1	**6001**		**WRITE TDR, READ RDR**
ACIA #2	**6002**		**WRITE CR, READ SR**
ACIA #2	**6003**		**WRITE TDR, READ RDR**
ACIA #3	**6004**		**WRITE CR, READ SR**
ACIA #3	**6005**		**WRITE TDR, READ RDR**
ACIA #4	**6006**		**WRITE CR, READ SR**
ACIA #4`	**6007**		**WRITE TDR, READ RDR**
Reserve	**6008**	**-**	**600F**
CPU SRAM	**6010**	**-**	**6FFF**

PROGRAM MODULE-

Memory Write Protect	**7000 WRITE**
I.D. Feature	**7000 READ**
I.D. Location	**7001 READ**
	7001 WRITE Reserve
Reserve	**7002 - 7009**
	700B - 700E WRITE
	700F READ
RTCA Valid/Reset	**700A**
RTCA Counters 1 to 4	**700B - 700E READ**
U3 Memory	**7010 - 7FFF**

U1 & U2 Memory 8000 - FFFF

Note -- Address locations noted as "Reserve" are assignable by the Agency only and shall not be used. CPU STATUS Bit 6: "0" equals Address Configuration 1 and "1" equals Address Configuration 2.

2.1.4.3
CONFIGURATION 2 Address Organization - This configuration provides all Model 412C Program Module features internal to the controller unit. The address organization is the same as CONFIGURATION 1 with the following exceptions:

CPU SRAM	**0000 - 3FFF**	**U3 & U4 Memory internal**
	6010 - 6FFF	
	7010 - 7FFF	
U6 EPROM	**8000 - FFFF**	**U1 & U2 Memory internal**

2.1.5
Each memory device shall stabilize to normal operation within 10 ms following Power Restoration and shall be in Standby until addressed. Each device shall have the following maximum power drain at +5 VDC in its various states:

MEMORY	ACTIVE	STANDBY	POWERDOWN
EPROM	100 ma	40 ma	-
SRAM	85 ma	20 ma	100 μa (non-internal power)

2.1.6
CPU EPROM MEMORY SOCKETS shall be a 28 Pin AMP Diplomate LF #641894-2, or equal. The MPU, ACIA and other memory sockets shall be an AUGAT #500/800 series AG10DPC or equal. Each socket number shall be permanently marked on the PCB adjacent to its Pin 1. Should the "... or equal MPU" Pin / Package be other than the 40 pin package, the MPU socket used shall match the above specified socket features.

CHAPTER 2 SECTION 2

MODEL 170E CONTROLLER UNIT

2.2.1 UNIT COMPOSITION

2.2.1.1
The Model 170E Controller Unit shall consist of the following:

- **Central Processing Unit (CPU)**
- **Input / Output Interface**
- **Unit Chassis**
- **M170E Auxiliary Board**
- **Model 412C Program Module**
- **Unit Power Supply with external power connection**
- **Unit Standby Power**
- **Front Panel Assembly**
- **Internal System Interface**
- **Connectors C1S, C2S, C20S, C30S, C40S, and T-1**
- **Communications System Interface**

2.2.1.2
The 170E shall be delivered pinned for Configuration 1 Addressing.

2.2.1.3
The composition weight shall not exceed 25 pounds.

2.2.2
CENTRAL PROCESSING UNIT (CPU)

2.2.2.1
The CPU shall be provided with an MPU and shall properly execute object programs developed to operate on the MPU. The MPU interrupt requirements shall be as follows:

2.2.2.1.1
Non-Maskable Interrupt (NMI) - The NMI is exclusively assigned to the Power Failure Function. A Power Failure shall cause the MPU NMI line to immediately go LOW. The line shall be held LOW until the RES goes LOW to prevent multiple NMI issuance.

2.2.2.1.2
Reset Interrupt (RES) - The RES is exclusively assigned to Power Restoration and MPU Startup. The RES line shall go LOW 3 (±1) ms following the NMI going LOW. The line shall remain LOW until 150 (±75) ms after Power Restoration.

2.2.2.1.3
Interrupt Request (IRQ) - The IRQ Line shall be jointly used by the RTC and Four ACIAs to initiate IRQ to the MPU.

2.2.2.1.3.1
Real Time Clock (RTC) - Real Time Clock circuitry shall be provided to trigger an interrupt to the MPU on the IRQ line once every 1/60 of a second during the 270 degree to 330 degree portion of the AC Sine Wave. The AC Sine Wave shall be derived from the local power company's 120 VAC 60 Hz frequency. The RTC shall be READ at Bit 8, Address 5FFF (STATUS) and reset by a WRITE to Address 5FFF.

2.2.2.1.3.2
ACIA - Four ACIAs shall be provided, each capable of receiving and transmitting up to eight-bits of parallel data from the MPU for serial data communications. The ACIA shall have 4 registers which are addressable by the MPU. The MPU shall be capable of reading the Status Register (SR) and the Receiver Data Register (RDR), and writing in the Transmit Data Register (TDR) and in the Control Register (CR).

2.2.2.1.3.3
Each ACIA shall be provided with a 2 post type jumper between its IRQ output and the MPU IRQ input. The 170E shall be delivered with these jumpers installed.

2.2.2.2
CPU Clock Timing - The CPU clock circuitry shall be provided to generate the MPU clock timing. The clock circuitry and the MPU shall provide two selectable MPU machine cycle times of 0.651 and 1.302 (±0.0015) μs. The machine cycle time selection shall be by Post Jumper (Three Post Type) with jumper in for 1.302 μs. The CPU clock circuitry shall be located no further than 50.80 mm from the MPU clock pin inputs.

2.2.2.3
SRAM Memory, DALLAS 1235Y or equal, shall be provided.

2.2.2.4
AN EPROM Memory, INTEL 24256A or equal, shall be provided in socket U6.

2.2.2.5
Restart Timer – A Restart Timer Circuitry shall be provided to react to the duration of power outage. The Restart Timer output is normally HIGH. When the NMI line goes LOW, the Restart Timer shall begin timing. If the timer reaches 1.75 (±0.25) seconds, its output state shall go to LOW and remain in that state for 50 (±24) ms after the RES line goes HIGH. If power is restored prior to the timer timing out, the output shall remain HIGH and the timer shall be reset to "0".

2.2.3
DOWNTIME ACCUMULATOR (DTA)

2.2.3.1
A DTA shall be provided to accumulate time between Power Failure and Restoration. The DTA shall start counting immediately upon NMI line going LOW and continue counting until the RES line goes HIGH following Power Restoration.

2.2.3.2
The DTA shall have 2 eight-bit binary registers counting the number of minutes and seconds. DTA accuracy shall be ±1 second over the 255-minute range. The DTA shall stop counting when the Minutes register equals 255 decimal. Both DTA registers shall reset to 0 by a WRITE to Address 5000. The DTA shall READ Minutes at Address 5000 and Seconds at Address 500F. The Seconds Register shall count 0 to 59 seconds decimal in 1-second increments. At 60 seconds, the Minutes Register shall be incremented and reset the other register to "0".

2.2.4
TOTAL CURRENT DRAIN FOR DTA AND RESTART TIMER CIRCUITRY (powerdown mode) shall not exceed 400 μa at 5 VDC, 35^0C while timing and 100 μa at 5 VDC when timeout is latches.

2.2.5
INPUT / OUTPUT INTERFACE

2.2.5.1
Input / Output Interface shall utilize a ground true logic. The transfer of data between interface and working registers within the MPU shall be in eight-bit word increments, minimum. The steering of data from inputs or outputs for a given address shall be controlled by the state of the MPU read / write command at the time the given address is valid.

2.2.5.2
Output Interface - The output interface shall consist of a minimum of 80 bits of buffered storage. Output data shall be latched at the time of writing from the MPU. This interface shall provide an NPN open collector output capable of driving up to 40 VDC and sinking up to 100 mA. A "1" from the MPU shall be presented as a grounded collector, and a "0" presented as an open circuit. Once a port is written into, the data shall remain present and stable until either another word is written into it or until the power is turned off. The state of these output ports at the time of power up or below power failure threshold shall be an open circuit.

2.2.5.3
Input Interface - The input interface shall consist of a minimum of 64 bits of gated inputs from external devices. Each logic level input shall be turned ON (true) when the input voltage is less than 3.5 VDC, shall be turned OFF (false) when the input current is less than 100 μa or the input voltage exceeds 8.5 VDC, shall pull up to 12 VDC, and shall not deliver in excess of 20 mA to a short circuit to logic level common. When the appropriate input address is impressed upon the input interface, the interface shall place its data on the data bus, which will be read by the MPU. Ground on any input shall be interpreted by the MPU as a "1" and an open on any input or the presence of a voltage greater than 8.5 VDC shall be interpreted as a "0" by the MPU when that input is read.

2.2.6
UNIT CHASIS - The controller unit shall be housed in a compact, portable metal enclosure suitably protected against corrosion. The controller unit shall mount in a standard EIA 19-inch rack. The enclosure shall be designed for convenient removal of PCBs without the use of tools.

2.2.7 UNIT POWER SUPPLY

2.2.7.1
A power supply shall be provided to produce all DC power necessary to operate the controller unit. In addition, the supply shall provide the following voltages and current:

1. 1000 mA at +12 VDC
2. 300 mA at -12 VDC
3. 500 mA at + 5 VDC
4. 400 mA at - 5 VDC

2.2.7.2
The DC ground shall not be connected to equipment ground.

2.2.7.3
Controller Unit power shall be held up (DC logic voltages at normal operating levels) for a minimum of 50 ±17 ms beyond the NMI line going LOW.

2.2.7.4
The maximum DC voltage generated shall not exceed 45 volts.

2.2.7.5
The Power Supply shall be so designed that no further filtering regulation is needed for the required DC voltages.

2.2.7.6
Radio frequency suppressors shall be provided on the AC+ and AC- power lines. The part shall be COR COM 3VS1 or equal.

2.2.8 UNIT STANDBY POWER

2.2.8.1
A standby power supply shall be provided to retain power (minimum of 72 hrs) to the CPU Restart Timer, DTA and Internal RTCA during power failure in the controller unit. The supply shall consist of holdup Capacitors, capacitor charging circuitry and power sense / transfer circuitry.

2.2.8.2
The power sense / transfer circuitry shall sense power loss and transfer battery power immediately to the required circuits. The transfer circuitry shall isolate the capacitors by

transistor or relay until power loss transfer. The circuitry shall sense power restoration and transfer back to the normal isolation mode.

2.2.8.3
A charging circuit which shall, under normal operating conditions, fully charge and float the standby capacitors consistent with manufacturer's recommendations.

2.2.9 FRONT PANEL ASSEMBLY

2.2.9.1
The front panel shall be securely fastened to the chassis and removable without the need for tools. A continuous hinge shall be provided on the left side of the unit to permit opening of the front panel and ready access to the interior of the controller unit.

2.2.9.2
The front panel shall be electrically connected by means of Connector C3. The front panel shall be connected to equipment ground through Connector C3.

2.2.9.3
The character displays shall be hexadecimal with circuits to accept, store, and display four-bit binary data. The characters shall be 10.16 mm high, minimum. Each character shall have latch strobe and blanking inputs. The second character from the right (lower row) shall have a right decimal point. The face of the character display shall be scratch and solvent-resistant. The transfer of data from the MPU through the output interface to the display shall result in the display of each character in its non-inverted state.

2.2.9.4
The front panel shall be provided with 10 LED CALL / ACTIVE indicators.

2.2.9.5
A keyboard shall be provided. The transfer of data from the keyboard by way of the input interface to the MPU shall result in each character being received in its non-inverted state. The character shall consist of 4 bits of binary data, while the character control shall consist of 1 bit. A low state on the character control to the interface shall indicate the presence of a valid character. Each key shall be engraved or embossed with its function character, shall have a minimum surface area of 48.39 mm^2 and shall be mounted on a minimum of 12.7 mm centers; shall have an actuation force between 50 and 100 grams and shall provide a positive tactical indication of contact. Key contacts shall have a design life of over one million operations, shall be rated for the current and voltage levels used, and shall stabilize within 5 ms following contact opening.

2.2.9.6
The front panel shall be provided with a toggle LOGIC switch to enable the stop timing function and shall be labeled "STOP TIMING".

2.2.9.7
An ON-OFF toggle CONTROL switch and fuse shall be provided for AC power. The switch and fuse shall protrude through the front panel, but shall remain with the controller unit chassis when the front panel is removed. The fuse shall be a 3AG Slow Blow type, rated at either 1 or 2 amperes, dependent upon the controller unit power requirements.

2.2.9.8
The front panel, under the legend "OPERATING INSTRUCTIONS", shall include a framework to retain a card, 101.60 mm wide by 152.40 mm high by 1.59 mm thick.

2.2.10 INTERNAL SYSTEM INTERFACE

2.2.10.1
PCB to PCB Connector spacing shall be a minimum of 25.4 mm. Continuous nylon card guides (permanent locking type) shall be provided for the modules and all internal PCBs.

2.2.10.2
Two PCB 22/44S Connectors shall be provided for the MODEM Modules MC1 and MC2, and two PCB 36/72S Connectors shall be provided for the M170 Connector / Program Module and the M170 Connector / M170E Auxiliary Board.

2.2.10.3
The depth placement of the vertical M/170 Connector shall be such that the Program Module Front Panel shall be flush with the Model 170E Controller Unit Front Panel when the module is connected.

2.2.11 DATA AND ADDRESS BUS REQUIREMENTS

2.2.11.1
All Data Bus Buffers and Data Bus Drivers shall be tri-state buffered devices enabling them to drive a load consisting of 10 TTL gates and 200 picofarads. The propagation delay time shall be less than 30 ns.

2.2.11.2
All Address Bus Inputs shall be buffered and shall load the bus by 1 TTL gate load and 100 picofarads.

2.2.12 CONNECTOR REQUIREMENTS

2.2.12.1
Connector C1S shall be mounted on the controller unit providing 44 inputs and 56 outputs of control interface to and from external devices or files.

2.2.12.2
The Model 400 MODEM and CPU ACIA connections into and out of the controller unit shall be made through Connector C2S, C20S, C30S, C40S, and Terminal Block T-1 (TYPE T Connector). The control and data transmission lines for ACIA 1 shall be paralleled

through C2S and T-1 connectors. ACIA 2 lines shall be routed to C20S Connector, ACIA 3 to C30S, and ACIA 4 to C40S.

2.2.12.3
ACIA 4 RS 232 Signal Lines and Buffered mirrored signals NMI, RES and ROT Shall be internally route to M170 and M170E as noted in Pin Assignments under Section 5 Details.

2.2.13 COMMUNICATION SYSTEM INTERFACE

2.2.13.1
The communication system shall consist of the CPU, ACIAs, motherboard connectors and lines, MODEM Module Connectors MC1 & MC2 and interfaces between ACIA & MODEM and both MODEM and ACIA to C2S, C20S, C30S, C40S and Connector / T-1 Terminal. The interface between the ACIA and MODEM shall comply with EIA RS-232-C Standards and all functions under T-1, C2, C20S, C30S, and C40S Connectors are referenced to the ACIA. AUDIO IN and AUDIO OUT are referenced to the MODEM. The RTS and TX Data lines to the MODEM shall have MARK and SPACE Voltages of -12 and +12 VDC respectively.

2.2.13.2
C20S, C30S, and C40S Connectors shall meet the requirements for the C2S Connector.

2.2.13.3
A minimum of four baud rate frequencies, 19.2 kHz, 38.4 kHz, 76.8 kHz and 153.6 kHz shall be provided at the ACIA Rx /Tx Clock Inputs (pins 3 & 4). The frequency selection shall be by post type jumpers. Each ACIA shall have independent baud rate selection with jumpers delivered pinned for 19.2 kHz.

2.2.14 ELECTRICAL REQUIREMENTS

2.2.14.1
The front panel and chassis shall be connected to equipment ground.

2.2.14.2
A surge arrestor shall be provided between the AC+ and AC- for protection against powerline noise transients. The surge arrestor shall meet the following requirements:

1. Recurrent peak voltage:	**212 Volts**
2. Energy rating maximum:	**20 Joules**
3. Power dissipation, average:	**0.85 Watt**
4. Peak current for pulses less than 6 us:	**2000 Amperes**
5. Standby current:	**less than 1 mA**

2.2.14.3
Two 0.5 ohm, 10 watt wire-wound power resistors with a 0.2µH inductance shall be provided (1 on the AC+ power line and 1 on the AC- line). Three surge arrestors rated for

20 Joules shall be supplied between AC+ and ground, AC- and ground, and between AC+ and AC-. A 0.68µF capacitor shall be added between AC+ and AC- coming off the 0.5 Ohm resistor going to the surge arrestors.

2.2.14.4
The AC power to the controller unit shall be supplied by a 3-conductor cable at least 3 feet in length. The cable shall terminate in a NEMA Type 5-15P grounding type plug.

2.2.14.5
Test points shall be provided for monitoring all power supply voltages. All test points shall be readily accessible when the front panel is opened. Any provided test point shall be isolated such that attaching a test probe shall not impact the operation of the controller unit. The test points shall be post type, 1.59 mm diameter and 4.76mm high, minimum. The clearance between test points and other components shall be 6.35 mm, minimum.

2.2.15 M170E AUXILIARY BOARD

2.2.15.1
The M170E Auxiliary Board shall contain the RTCA Circuitry and the Identification Switches. (See Section 3 for the RTCA circuitry and the Identification Switch requirements.) The RTCA circuitry and the Identification Switches on the M170E Auxiliary Board shall be disabled when a Model 412C is installed. The M170 connector pins 71 and / or 72 shall provide a DC Ground path via the Model 412C Module (pins 69 & 70) to M170E connector (pins 71 & 72). A ground true present shall cause board feature disablement.

2.2.15.2
The M170E Auxiliary Board's PCB dimensions shall be identical to the Model 400 Modem except for the PCB edge connector dimensions.

2.2.15.3
The M170E Auxiliary Board's PCB connector shall be a PCB 36 / 72 and shall mate with the M170E connector.

CHAPTER 2 SECTION 3

MODEL 400 MODEM MODULE

2.3.1
The MODEM shall provide two-wire half-duplex and four-wire full-duplex communications. It shall be switch selectable between half duplex and full duplex. In half duplex, pins X and Y shall be used for Audio IN / OUT.

2.3.2
The MODEM shall be compatable with Bell Standard 202S and comply with the following requirements:

2.3.2.1
Data Rate: 300 to 1200 baud modulations.

2.3.2.2
Modulation: Phase coherent frequency shift keying (FSK).

2.3.2.3
Data Format: Asynchronous, serial by bit.

2.3.2.4
Line and Signal Requirements: Type 3002 voice-grade, unconditioned.

2.3.2.5
ACIA and MODEM Interface: EIA - 232 Standards.

2.3.2.6
Tone Carrier Frequencies (Transmit & Receive): 1200 Hz (MARK) and 2200 Hz (SPACE) with ±1% tolerance. The operating band shall be (half power, -3dB) between 1000 and 2400 Hz.

2.3.2.7
Transmitting Output Signal Level: 0, -2, -4, -6 and –8 dB (at 1700 Hz) continuous or switch selectable.

2.3.2.8
Receiver Input Sensitivity: 0 to –40 dB.

2.3.2.9
Receiver Bandpass Filter: Shall meet the error rate requirement and shall provide 20 dB/Octave, minimum active attenuation for all frequencies outside the operating band.

2.3.2.10
Clear-to-Send (CTS) Delay: 12 (±2) ms.

2.3.2.11
Receive Line Signal Detect Time: 8 (±2) ms mark frequency.

2.3.2.12
Receive Line Squelch: 6.5 (±1) ms, 0 ms (OUT).

2.3.2.13
Soft Carrier (900 Hz) Turn Off Time: 10 (±2) ms.

2.3.2.14
MODEM Recovery Timer: Capable of receiving data within 22 ms after completion of transmission.

2.3.2.15
Error Rate: Shall not exceed 1 bit in 100,000 bits, with a signal-to-noise ratio of 16 dB measured with flat-weight over a 300 to 3000 Hz band.

2.3.2.16
Transmit Noise: Less than –50 dB across 600 ohm resistive load within the frequency spectrum of 300 to 3000 Hz at maximum output.

2.3.3
The MODEM power requirements are as follows:

Input Voltage	Maximum Current Consumption
+12 VDC	75 Milliamperes
-12 VDC	75 Milliamperes

2.3.4
Indicators shall be provided on the front of the MODEM to indicate Carrier Detect, Transmit Data, and Receive Data.

CHAPTER 2 SECTION 4

MODEL 412C PROGRAM MODULE

2.4.1 GENERAL REQUIREMENTS

2.4.1.1
A device shall be provided to prevent the module, when inserted upside down, from making contact with the modules' mating connector within the controller unit.

2.4.1.2
The module PCB Connector shall be provided with electrostatic discharge protection to prevent CMOS device damage.

2.4.1.3
The VMA / Phase 2 (E) Clock Signal (M/170 Pin 25) shall not be used in a memory device READ operation.

2.4.1.4
The total module current requirements shall not exceed 450 mA at +12 VDC and 100 mA at +5 VDC.

2.4.1.5
Address 700E, Bit 8 shall permanently Read as "1". This bit state is used to differentiate between past delivered Model 412/64 modules (Bit 8 decoded "0") and the Model 412C module.

2.4.1.6
The module PCB connector shall be a PCB 36/72P.

2.4.1.7
The module front panel shall be connected to Equipment Ground at M170 Pin 34.

2.4.1.8
All addressable devices shall be fully decoded.

2.4.1.9
All memory sockets shall be a 28 pin AUGAT #528/828 Series AG10DPC or equal.

2.4.2 FEATURE REQUIREMENTS

2.4.2.1 BUS INPUTS AND OUTPUTS

2.4.2.1.1
All data lines shall be tri-state buffered on the module enabling them to drive a load consisting of 10 TTL gates and 200 picofarads. When this module is not being addressed,

the data output lines shall be disabled into a high impedance state and the data lines shall not source or sink more than 100 µA.

2.4.2.1.2
All addressed input lines shall load the bus by 1 TTL gate load and 100 picofarads. The propagation delay time shall be less than 30 ns.

2.4.2.2 MEMORY

2.4.2.2.1
Four numbered memory sockets shall be provided and fully decoded using the following method. The module shall be delivered with MEMORY SELECT #3 Configuration designated memory devices (OR EQUAL), address decode and jumpers.

2.4.2.2.2
Device manufacturer is designated as INT-Intel, D-Dallas and HD-Hitachi. The sockets shall be decoded by block jumper selection as follows:

MEMORY SELECT	SOCKET ADDRESS RANGE AND DEVICE				JUMPER PATTERN		
	U1	U2	U3	U4	1	2	3
1	E000-FFFF INT2764A	C000-DFFF INT2764A	7010-7FFF DAL1225	1000-4FFF HD6264 OR HD62256	IN	IN	OUT
2	C000-FFFF INT128A	8000-BFFF INT128A	SAME	SAME	OUT	IN	IN
3	8000-FFFF	NOT ADRS	SAME	SAME *	OUT	OUT	IN
4	8000-FFFF INT27256A	3000-4FFF DAL1225	SAME	1000-2FFF SAME *	OUT	OUT	OUT

*** The pin #26 jumper pattern shall provide either address line 13 for the HD62256 device or tied HIGH for CS2 function in HD6264. Pin 27 shall be assigned to WE function.**

2.4.2.2.3
Jumper positions for Sockets U2 and U4 shall be provided to convert the sockets from an EPROM socket to a SRAM socket or vice versa. Jumper positions for Sockets U2, U3 and U4 shall be provided to convert the socket from a non-standby power socket to a standby power socket or vice versa. Sockets U2 and U3 shall be jumpered for non-standby power. Socket U4 shall be jumpered for standby power.

2.4.2.2.4
A Write Protect Circuit (WPC) shall be provided to prevent writing to SRAM memory during the Controller Unit MPU RESET Interrupt Line in a LOW State. A WRITE to ADDRESS 7000 shall be decoded and shall activate the WPC to place the R/W in a READ

ONLY State. A subsequent WRITE to ADDRESS 7000 shall be decoded and shall deactivate the WPC allowing R/W function. The WPC state shall be brought out to Address 700E, Bit 7 ("1" State means "active"). The WPC power drain shall not exceed 40 µA at +5 VDC.

2.4.2.3 MODULE POWER SUPPLY

2.4.2.3.1
A power supply shall be provided onboard the module consisting of a DC Regulation Circuit, Standby Power and all necessary support circuitry.

2.4.2.3.2
A DC Regulator device with its circuitry shall be provided to reduce the +12 VDC to +5 VDC for module use. The Regulator shall have a minimum efficiency of 75% and provide +5 ±0.25 VDC from no load to full load with a maximum of 2% ripple.

2.4.2.3.3
Standby power shall be provided to holdup WPC, SRAM and RTCA circuits during a Model 170 Controller Unit Power Failure. A circuit shall be provided to sense the +12 VDC M/170 power line and switch to standby power when the line falls below +9 VDC. The standby power circuit shall switch off when the power line is greater than +11 VDC. The standby power shall be a standard "AA" cap terminal cell battery rated at a minimum of 1.6 Ampere-hours at 3.7 ±0.2 VDC. All module circuitry and devices shall not exceed a maximum power drain of 2 mA at 3.7 VDC on the Standby Battery.

2.4.2.3.4
The battery shall be delivered separate from the module. It shall not be used except for test loading check by the Contractor.

2.4.2.3.5
A battery holder for a "AA" battery shall be provided securely mounted to the back of the front panel. The holder shall have a TAB header type connector attached to the battery plus mounting terminal.

2.4.2.4 IDENTIFICATION SWITCH CIRCUITRY

2.4.2.4.1
Two identification switch packages and associated circuitry shall be provided. The switch packages shall be decoded at Address 7000 (features) and 7001 (locations). Each package shall have 8 SPST switch positions with each switch associated to a DATA Bit (Switch 1 to Bit 1 and so on). Switch ON shall denote bit state "1" to the 170 CPU and Switch OFF shall denote bit state "0" to the 170 CPU.

2.4.2.4.2
The Switch Package shall be a DIP slide type and shall have recessed switches to prevent accidental switching.

2.4.2.5 REAL TIME CLOCK AJUSTER (RTCA)

2.4.2.5.1
A RTCA shall be provided to adjust for missing RTC timing interrupts.

2.4.2.5.2
The RTCA shall be continuously powered and not affected by a controller unit power failure. RTCA accuracy shall be ±10 ppm at 25^0C. Integral devices incorporating RTCA features and functions may be used in lieu of individual components. The RTCA current drain shall not exceed 1.5 mA at +3.7 VDC.

2.4.2.5.3
The RTCA shall include a free running 60 Hz Pulse Generator (PG), a 24 bit binary counter counting 60 Hz pulses, 4 eight-bit buffer ports and port decode / PG interrupt logic. The PG shall trigger binary counter to increment on every input pulse, counting continuously until reset to 0 by its Reset Line. Bits 21, 22, 23 and 24 in an all "1"'s state shall cause that PG to be disabled (Binary Counter Bit 1 is the least significant bit).

2.4.2.5.4
The counter bits shall be continuously read out to 4 eight-bit buffer ports. The ports shall be addressed and bits assigned as follows:

CPU ADDRESS	PORT BITS	COUNTER BITS	COMMENTS
700A	This address shall normally READ (decode) "55 HEX". If the standby power supply fails or is removed, it shall decode "54 HEX". A WRITE to this address will RESET the RTCA Binary Counter.		
700B	1-6	1-6	READ Only
700C	1-6	7-12	READ Only
700D	1-6	13-18	READ Only
700E	1-6	19-24	READ Only

2.4.2.5.5
A SPST finger throw LOGIC switch shall be provided on the board to activate/deactivate standby power to the RTCA Circuitry. With the switch in the deactivated state the RTCA Circuitry shall present NO power drain to the standby power supply.

CHAPTER 2 SECTION 5

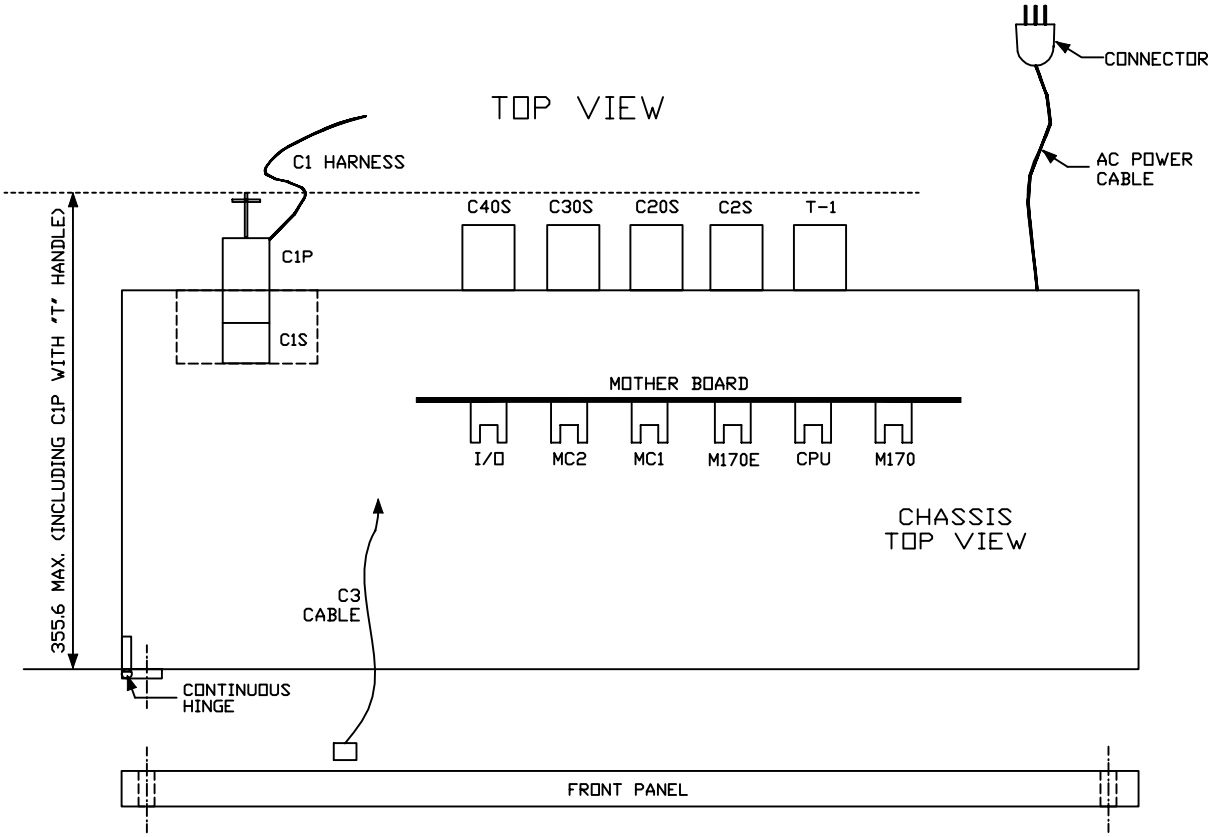
CHAPTER DETAILS

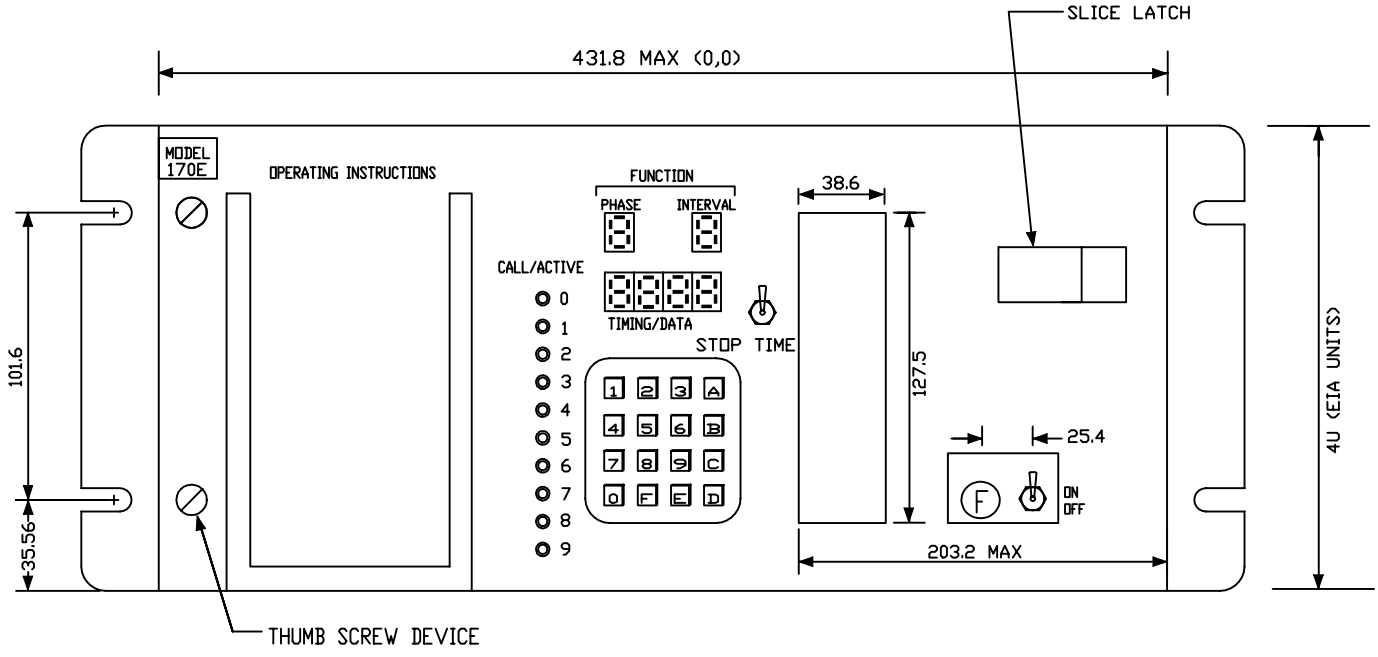
NOTES:

1. **All dimensions shall be in millimeters.**
2. **Program module' height and width dimensions are maximum.**
3. **C1 connector Pins 1, 14, 92 & 104 shall be connected to the controller unit DC logic ground.**
4. **All function under connector C2 & the terminal block T-1 are in reference to the MODEM**
5. **Detail Definitions:**

   BL = BLANKING
   CC = CHARACTER CONTROL OR STROBE
   CD = CARRIER DETECT
   CH = CHARACTER
   CTS = CLEAR TO SEND
   DP = DECIMAL POINT
   LS = LEAST SIGNIFICANT
   MS = MOST SIGNIFICANT
   NA = PRESENTLY NOT ASSIGNED. CANNOT BE USED BY THE CONTRACTORS FOR OTHER PURPOSES.
   NLS = NEXT LEAST SIGNIFICANT
   NMS = NEST MOST SIGNIFICANT
   P&I = PHASE AND INTERVAL
   RTS = REQUEST TO SEND

MODEL 170E CONTROLLER UNIT DIAGRAM



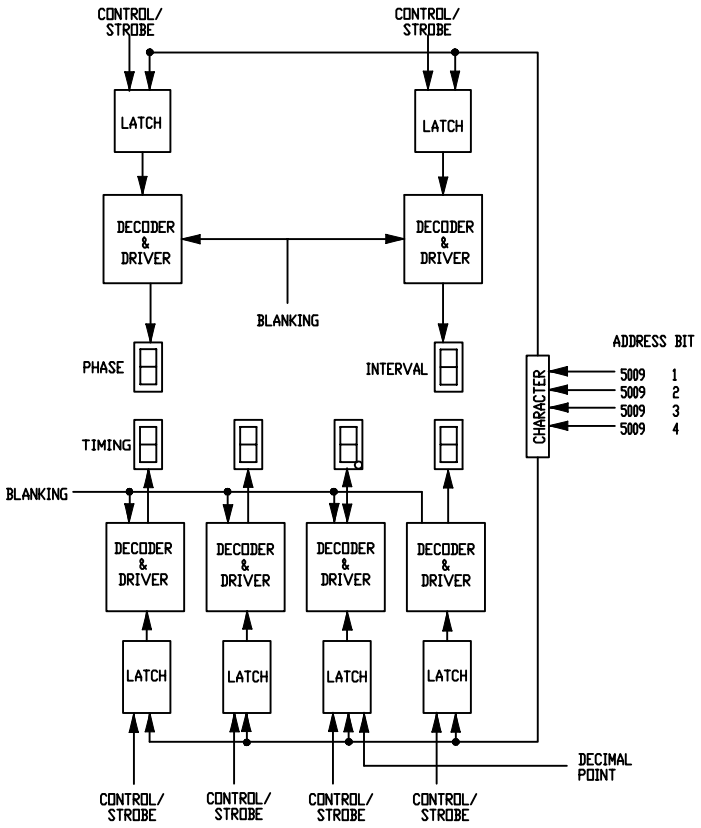


FRONT PANEL DISPLAY AND UNIT DETAIL

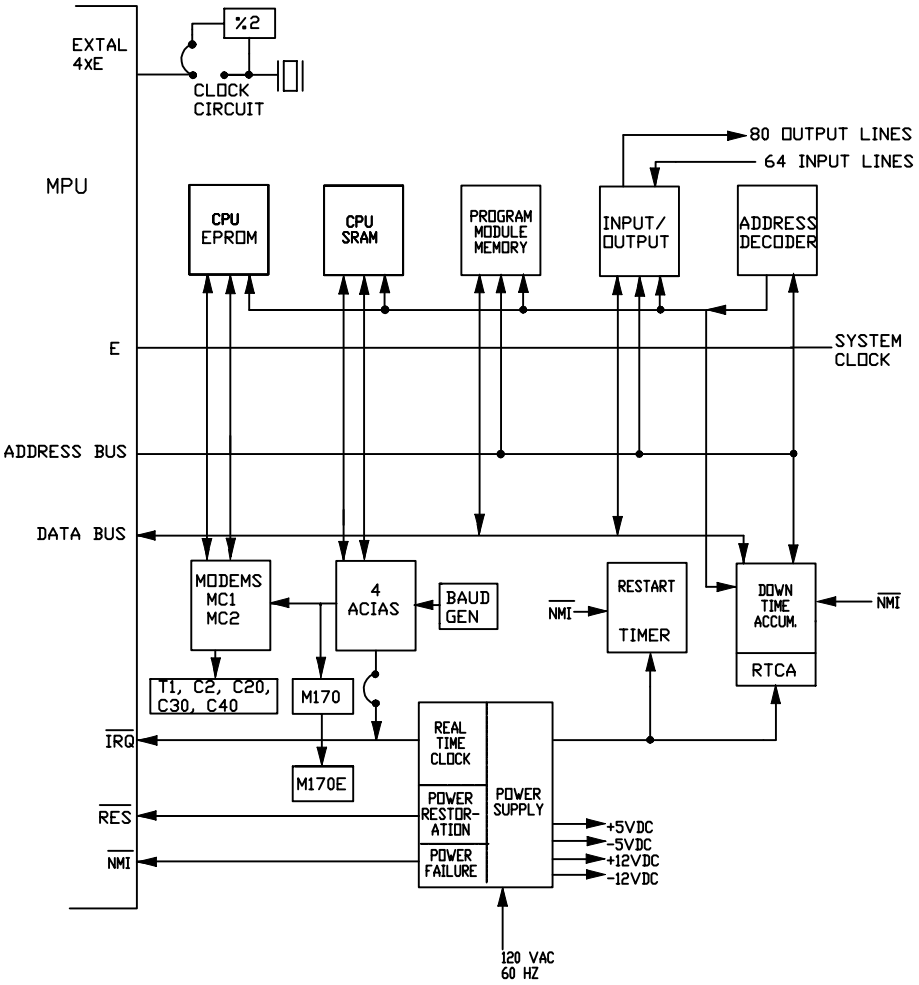
TITLE: MODEL 170E CONTROLLER UNIT DIAGRAM		
	NO SCALE	
	MARCH 29, 2002	2-5-1

MODEL 170E CONTROLLER UNIT BLOCK DIAGRAMS

FRONT PANEL DISPLAY BLOCK DIAGRAM



ORGANIZATION OF MODEL 170E CONTROLLER UNIT BLOCK DIAGRAM



TITLE:

MODEL 170E CONTROLLER UNIT BLOCK DIAGRAMS

NO SCALE

MARCH 29, 2002

2-5-2

INPUT PORT ADDRESS ASSIGNMENTS FOR CONNECTORS C1 AND C3

INPUT PORT ADDRESS	BIT	CONNECTOR C1 C3 SOCKET CONTACTS	INPUT PORT ADDRESS	BIT	CONNECTOR C1 C3 SOCKET CONTACTS	
5001	1	39	5005	1	67	
5001	2	40	5005	2	68	
5001	3	41	5005	3	69	
5001	4	42	5005	4	70	
5001	5	43	5005	5	71	
5001	6	44	5005	6	72	
5001	7	45	5005	7	73	
5001	8	46	5005	8	74	
5002	1	47	5006	1	75	
5002	2	48	5006	2	76	
5002	3	49	5006	3	77	
5002	4	50	5006	4	78	
5002	5	51	5006	5	79	
5002	6	52	5006	6	80	
5002	7	53	5006	7	81	
5002	8	54	5006	8	82	
5003	1	55	5007	1		KEYBOARD CONTROL
5003	2	56	5007	2		KEYBOARD CH LS
5003	3	57	5007	3		KEYBOARD CH NLS
5003	4	58	5007	4		KEYBOARD CH NMS
5003	5	59	5007	5		KEYBOARD CH MS
5003	6	60	5007	6		STOP TIMING
5003	7	61	5007	7		NA
5003	8	62	5007	8		NA
5004	1	NA	5008	1		NA
5004	2	NA	5008	2		NA
5004	3	NA	5008	3		NA
5004	4	NA	5008	4		NA
5004	5	63	5008	5		NA
5004	6	64	5008	6		NA
5004	7	65	5008	7		NA
5004	8	66	5008	8		NA

CONNECTOR C2 SOCKET ASSIGNMENT (C20, C30 & C40)

C2 SOCKET CONTACTS	FUNCTION	C2 SOCKET CONTACTS	FUNCTION
A	Audio IN	J	RTS
B	Audio IN	K	Data IN
C	Audio OUT	L	Data OUT
D	+5VDC	M	CTS
E	Audio OUT	N	DC GND
F	-5VDC	P	NA
H	CD	R	NA

TERMINAL BLOCK T-1 ASSIGNMENTS

1. Audio IN
2. Audio IN
3. CD
4. RTS
5. Data IN
6. CTS
7. Data Out
8. Audio Out
9. Audio Out
10. DC GND

TITLE:

MODEL 170E INPUT ADDRESS

NO SCALE

MARCH 29, 2002

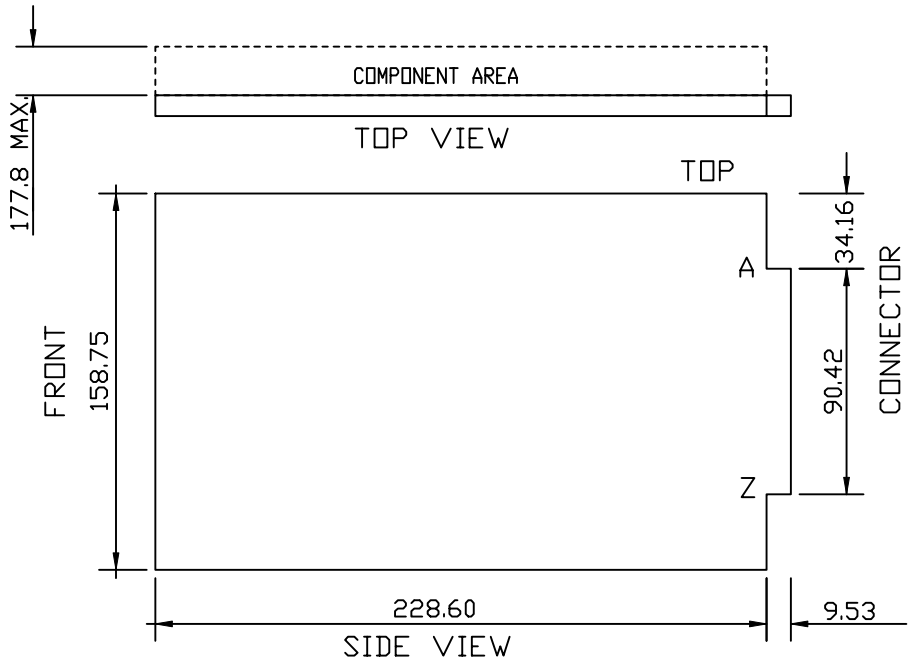
2-5-3

OUTPUT PORT ADDRESS ASSIGNMENTS FOR CONNECTORS C1 AND C3

OUTPUT PORT ADDRESS	BIT	CONNECTOR C1 SOCKET CONTACTS	OUTPUT PORT ADDRESS	BIT	CONNECTOR C1 SOCKET CONTACTS	C3
5001	1	2	5006	1	83	
5001	2	3	5006	2	84	
5001	3	4	5006	3	85	
5001	4	5	5006	4	86	
5001	5	6	5006	5	87	
5001	6	7	5006	6	88	
5001	7	8	5006	7	89	
5001	8	9	5006	8	90	
5002	1	10	5007	1	91	
5002	2	11	5007	2	93	
5002	3	12	5007	3	94	
5002	4	13	5007	4	95	
5002	5	15	5007	5	96	
5002	6	16	5007	6	97	
5002	7	17	5007	7	98	
5002	8	18	5007	8	99	
5003	1	19	5008	1		CC-PHASE
5003	2	20	5008	2		CC-INTERVAL
5003	3	21	5008	3		CC-TIMING LS
5003	4	22	5008	4		CC-TIMING NLS
5003	5	23	5008	5		CC-TIMING MLS
5003	6	24	5008	6		CC-TIMING MS
5003	7	25	5008	7		CALL LT 8
5003	8	26	5008	8		CALL LT 9
5004	1	27	5009	1		CH-LS
5004	2	28	5009	2		CH-NLS
5004	3	29	5009	3		CH-NMS
5004	4	30	5009	4		CH-MS
5004	5	31	5009	5		DP
5004	6	32	5009	6		BL-P&I
5004	7	33	5009	7		BL-TIMING
5004	8	34	5009	8		NA
5005	1	35	500A	1		CALL LT 0
5005	2	36	500A	2		CALL LT 1
5005	3	37	500A	3		CALL LT 2
5005	4	38	500A	4		CALL LT 3
5005	5	100	500A	5		CALL LT 4
5005	6	101	500A	6		CALL LT 5
5005	7	102	500A	7		CALL LT 6
5005	8	103	500A	8		CALL LT 7

TITLE: OUTPUT PORT ADDRESS ASSIGNMENTS FOR CONNECTORS C1 & C3		
	NO SCALE	
	MARCH 29, 2002	2-5-4

MODEL 400 MODEM MODULE



MODEL 400 MODULE CONNECTOR ASSIGNMENT

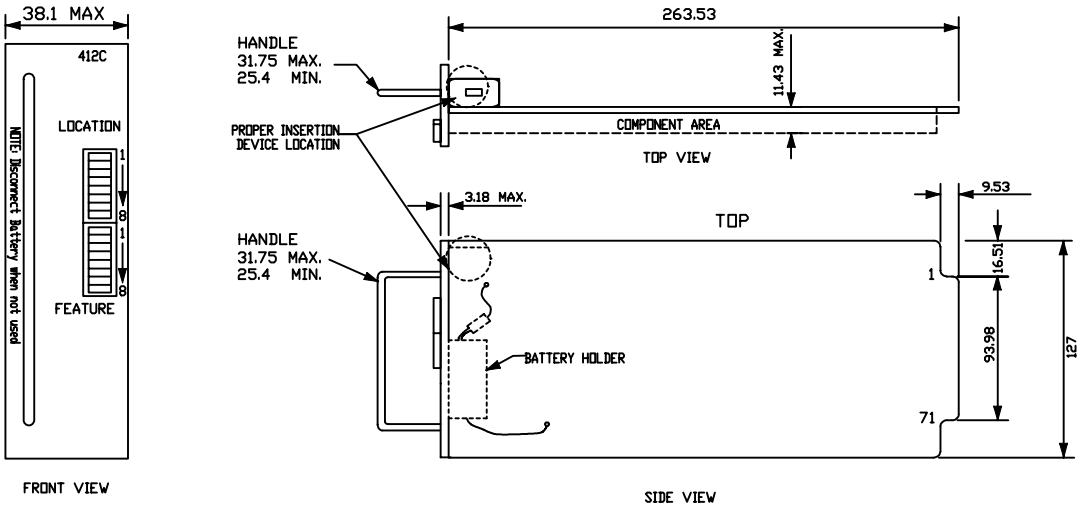
COMPONENT SIDE		CIRCUIT SIDE	
CONTACT	MODEL 400 FUNCTION	CONTACT	MODEL 400 FUNCTION
1	NA	A	DC GROUND
2	AUDIO INPUT	B	DC GROUND
3	AUDIO INPUT	C	12 VDC
4	NA	D	12 VDC
5	NA	E	-12 VDC
6	NA	F	-12 VDC
7	NA	H	NA
8	NA	J	NA
9	NA	K	CARRIER DETECT
10	NA	L	REQUEST TO SEND
11	NA	M	DATA INPUT
12	NA	N	CLEAR TO SEND
13	NA	P	DATA OUTPUT
14	NA	R	NA
15	NA	S	NA
16	NA	T	NA
17	NA	U	NA
18	NA	V	NA
19	NA	W	NA
20	NA	X	AUDIO OUTPUT
21	NA	Y	AUDIO OUTPUT
22	NA	Z	NA

TITLE:

MODEL 400 MODEM MODULE

	NO SCALE	
	MARCH 29, 2002	2-5-5

MODEL 412C PROGRAM MODULE AND CONNECTORS M170 & M170E



M170, M170E, AND 412C
PROGRAM MODULE CONNECTOR ASSIGNMENTS

CIRCUIT SIDE		COMPONENT SIDE		M170 ONLY
FUNCTION	PCB CONNECTOR		FUNCTION	NOT REQUIRED BY 412C
A0	1	2	A1	
A2	3	4	A3	
A4	5	6	A5	
A6	7	8	A7	
A8	9	10	A9	
A10	11	12	A11	
A12	13	14	A13	
A14	15	16	A15	
$\overline{D0}$	17	18	$\overline{D1}$	
$\overline{D2}$	19	20	$\overline{D3}$	
$\overline{D4}$	21	22	$\overline{D5}$	
$\overline{D6}$	23	24	$\overline{D7}$	
$\overline{VMA}$ / Q2(E)	25	26	NA	RES
READ/WRITE	27	28	NA	NMI
NA	29	30	NA	ROT
NA	31	32	NA	
NA	33	34	EQUIP. GND	
NA	35	36	NA	RTS ACIA 4
NA	37	38	NA	CTS ACIA 4
NA	39	40	NA	DCD ACIA 4
NA	41	42	NA	TXD ACIA 4** (SEE NOTE)
NA	43	44	NA	RXD ACIA 4** (SEE NOTE)
NA	45	46	NA	
NA	47	48	NA	
NA	49	50	NA	
NA	51	52	NA	
NA	53	54	NA	
NA	55	56	NA	
NA	57	58	NA	
12 VDC	59	60	12 VDC	
-12 VDC	61	62	-12 VDC	
	KEY			
-5 VDC	63	64	-5 VDC	
5 VDC	65	66	5 VDC	
5 VDC	67	68	5 VDC	
GND	69	70	GND	
GND	*71	*72	GND	

* PINS 71 & 72 ON M170 & M170E CONNECTORS SHALL BE COMMONED. PINS 71 & 72 ON THE MODEL 412C SHALL BE TIED TO PINS 69 & 70.

** RELATIVE TO THE ACIA

TITLE:
MODEL 412C PROGRAM MODULE AND CONNECTORS M170 & M170E

NO SCALE

MARCH 29, 2002

2-5-6

CHAPTER 3

SPECIFICATIONS FOR AUXILIARY CABINET UNITS

TABLE OF CONTENTS

CHAPTER 3 SECTION 1

GENERAL REQUIREMENTS

3.1.1 MODELS 200 AND 204 GENERAL

3.1.1.1
The unit chassis shall be made of metal suitable to meet rigid support and environmental requirements. Where electrical isolation is the only requirement, plastic insulation material can be used in lieu of metal.

3.1.1.2
The unit control circuitry and switches shall be readily accessible by the use of a screwdriver or wrench. Only one type of screw head end (Slotted or Phillips) shall be used.

3.1.1.3
The unit shall be so constructed that no live voltage is exposed. A handle shall be attached to the front panel for insertion or removal from the unit mating connector.

3.1.1.4
The unit shall be so constructed that its lower surface shall be no more than 52.34 mm below the centerline of the connector and no part shall extend more than 22.86 mm to the left or 27.94 mm to the right of the connector centerline.

3.1.1.5
Continuous edge guides shall be provided on the unit.

3.1.1.6
Each switch shall be capable of switching any Current from 0.050 to 10.0 Amperes (AC) load with power factor of 0.85 or higher.

3.1.1.7
Each switch shall be designed for a minimum of 300 Million operations while switching a tungsten load of 1000 Watts at 70 degrees C. Switch isolation between DC input and AC output circuit shall be at least 10,000 meg-ohms at 2000 VDC.

3.1.1.8
Unit indicators shall be vertically centered on the front panel with indicators positioned no more than 25.3 mm from said center.

3.1.2
MODEL PLUG CONNECTORS SHALL BE:

Model 200	**BEAU P 5412 - LAB or equal**
Model 204	**BEAU P 5406 - LAB or equal**

CHAPTER 3 SECTION 2

MODEL 200 SWITCH PACK UNIT

3.2.1
The Model 200 Switch Pack Unit shall be a modular plug-in device containing three solid-state switches. Each switch shall open or close a connection between applied power and external load.

3.2.2
A Ground True Controller Unit Input (0 to 6 VDC) shall cause the switch to energize and a Ground False (16 VDC or more) shall cause it to de-energize, State transition shall occur between 6 and 16 VDC. The input shall not sink more than 20 ma or be subjected to more than 39 VDC. The input shall have reverse polarity protection.

3.2.3
With all switches on, the unit shall not draw more than 60 ma at +16 VDC or more from the +24 VDC cabinet supply.

3.2.4
Each switch shall have an OFF state dv/dt rating of 100 V/μs or better. Each switch shall be isolated so that line transients or switch failure shall not alter the controller unit.

3.2.5
The unit front panel shall have an indicator on the input to each switch. The indicator shall be labeled or color-coded "Red"-top switch, "Yellow"-middle switch, and "Green"-bottom switch. The middle switch indicator shall be vertically centered on the unit front panel with the other indicators positioned 25.4 mm above and below.

3.2.6
The resistance between the AC+ input terminal and the AC+ output terminal of each switch shall be a minimum of 15,000 ohms when the switch is in open state. When the switch is in off state the output current through the load shall not exceed 20 mA peak.

CHAPTER 3 SECTION 3

MODEL 204 - FLASHER UNIT AND

MODEL 205 – FLASH TRANSFER RELAY UNIT

3.3.1 MODEL 204 FLASHER UNIT

3.3.1.1
The FTR shall be a modular plug-in device containing a flasher control circuit and two solid-state switches. The unit's function is to alternatively open and close connections between applied power and external load.

3.3.1.2
The unit shall generate its own internal DC power from the AC Line.

3.3.1.3
The unit shall commence flashing operation when AC power is applied providing 50 to 60 flashes per minute per switch with a 50 % duty cycle.

3.3.1.4
Each switch shall have an OFF state dv /dt rating of 200 V/μs or better.

3.3.1.5
An indicator showing the switch's output state shall be provided.

3.3.1.6
Each circuit shall be designed to operate in an open-circuit condition without load for 10 years minimum.

3.3.1.7
A surge arrestor shall be provided between AC (pin 11) and Flasher Output (pins 7 & 8). The arrestor shall meet the following requirements:

Recurrent Peak Voltage	**212 Volts**
Maximum Energy Rating	**50 Joules**
Average Power Dissipation	**0.85 Watts**
Peak I for pulses less than 6 us	**2000 Amperes**
Standby I	**less than 1 mA**

3.3.2 MODEL 205 FLASH TRANSFER RELAY UNIT

3.3.2.1
The relay unit shall be of electromechanical type, designed for continuous duty:

3.3.2.2
Each unit shall be enclosed in a removable, clear plastic cover. The manufacturer name, its electrical rating, and part number shall be placed on the cover. They shall be durable, permanent and readily visible.

3.3.2.3
Each unit shall be provided with DPDT contacts. The contact points shall be of fine silver, silver alloy or a superior alternate material. Contact points and arms shall be capable of switching 20 Amperes or 1 Kilowatt Tungsten Load at 120 VAC per contact at least 100,000 operations without contact welding or excessive burning, pitting or cavitation. The points and arms shall be able to withstand 0.1 DA or 10 Gs, 10 –55 HZ without contact chatter.

3.3.2.4
The relay coil shall have a power consumption of 2.0 Volt - Ampere maximum.

3.3.2.5
Each relay shall withstand a potential of 1500 VAC at 60 Hz between insulated parts and between current carrying or non-carrying parts. Each relay shall have a one cycle surge rating of 175 Amperes RMS and pickup and drop out within 20 ms.

CHAPTER 3 SECTION 4

MODEL 206 T170 POWER SUPPLY UNIT

3.4.1
The unit chassis shall be vented. The power supply cage and transformers shall be securely braced to prevent damage in transit. When resident in the PDA, the units shall be held firmly in place by its stud screws and wing nut.

3.4.2
The unit shall provide +24 VDC to the cabinet files. The unit shall be of ferro-resonant design. It shall have no active components and conform to the following requirements:

3.4.2.1
Input Protection - Two 0.5 ohm, 10-watt wire-wound power resistors with a 0.2 µh inductance shall be provided (one on the AC+ Line & on the AC- Line). Three 20 Joule surge arrestors shall be provided between AC+ to AC, AC+ to EG, and AC- to EG. A 0.68 µf. capacitor shall be placed between AC+ & AC- (between the resistors & arrestors).

3.4.2.2
Line and load regulation shall meet the power supply range for +24 VDC (23.0 to 26 VDC). This includes ripple noise; from 90 to 135 VAC at 60 Hz., plus an additional 1.6% for each additional 1.0% frequency change; and current range from 1 to 5 Amperes with a maximum temperature rise of 30 degrees C above ambient.

3.4.2.3
Design Voltage - +24 +/- 0.5 VDC at full load, 30 degrees C, 115 VAC incoming after a 30-minute warm-up period.

3.4.2.4 Full Load Current 5 AMPS each for +24 VDC, minimum.

3.4.2.5 Ripple Noise - 2 volts peak-to-peak and 500 millivolts RMS at full load.

3.4.2.6 Efficiency - 70% minimum.

3.4.2.7 Circuit capacitors shall be rated for 40 volts minimum.

3.4.3
The front panel shall include AC and DC fuses, power ON light and test points for monitoring the output voltages. The unit including terminals shall be protected to prevent accidental contact with energized parts.

CHAPTER 3 SECTION 5

MODEL 208 T170 MONITOR UNIT

3.5.1
The Model 208 Monitor Unit shall reliably sense and cause a relay output contact (FAILED STATE) when monitoring the following:

1. **A WDT Timeout Condition**
2. **Cabinet +24 VDC Power Supply below specified threshold**

3.5.2
WatchDog Timer Requirements

3.5.2.1
WDT Circuitry shall be provided to monitor a controller unit output line state routed to the monitor unit at its assigned pin. The WDT Circuitry shall sense any line state change and the time between the last change. No state change for 1.5 ± 0.1 seconds shall cause a FAILED state. The timer shall reset at each state change in a NON FAILED state.

3.5.2.2
Only the Unit Reset or a WDT inactive due to the voltage sense shall reset the WDT from a FAILED state.

3.5.2.3
A FAILED state caused by the WDT shall illuminate a front panel indicator light labeled "WDT ERROR". The indicator shall remain ON until Unit Reset Issuance.

3.5.2.4
The WDT Circuitry shall sense the incoming VAC Line and when the voltage falls below 98 ± 2 VAC for 50 ± 17 ms shall inhibit the WDT Function. When the WDT Circuitry senses the incoming VAC Line rise above 103 ± 2 VAC for 50 ± 2 ms the WDT shall become active. A hysteresis between the Voltage Inhibit and the Voltage Active Settings shall be a minimum of 3 Volts.

3.5.3
Power Supply Monitor Requirements

3.5.3.1
The monitor unit shall sense the Cabinet +24 VDC Power Supply Output Voltage. Voltages sensed at +18 VDC or below for a duration of 500 ms or longer shall cause a FAILED state. Voltages sensed at +22 VDC or above shall NOT cause a FAILED state. Voltages sensed below +22 VDC for a duration of 200 ms or less shall NOT cause a FAILED state. All timing and voltages conditions other than those specified above may or may not cause a FAILED state.

3.5.3.2
A FAILED state caused by sensing the power supply shall illuminate a front panel indicator light labeled "VDC FAILED". The indicator shall remain ON until Unit Reset.

3.5.3.3
Only Unit Reset shall reset the power supply sense circuitry from a FAILED state.

3.5.4
FAILED State Output Circuits
An electro-mechanical relay shall be provided to switch an output circuit during a FAILED state. The relay coil shall be energized in a NON FAILED State. The relay contacts shall be rated for a minimum of 3 amperes at 120 VAC and 100,000 operations. Contact opening/closing time shall be 30 ms or less.

3.5.5
Monitor Unit Reset
A momentary SPST CONTROL switch labeled "RESET" shall be provided on the unit front panel to reset the monitor unit circuitry to a NON FAILED state. The switch shall be so positioned on the front panel that the switch can be operatied while gripping the front panel handle.

3.5.6
The unit shall be provided with provision to drive an external NE2H light through a 56 KOhm, 1/2 Watt series restor (resident on unit).

3.5.7
The PDA #3 WDT Reset Input shall not be sensed by the unit.

3.5.8
The output relay CONTACT FOR FAILED STATE shall be OPEN

CHAPTER 3 SECTION 6

MODEL 210 T170 MONITOR UNIT

3.6.1
The Monitor Unit shall sense the following conditions and cause a FAILED STATE should any of the conditions exist:

1. **The cabinet +24 VDC power supply below the voltage threshold.**
2. **The WDT Timeout Condition.**
3. **Conflicting field Output Circuit ON Condition.**

3.6.2
See Chapter 3, Section 5 Model 208 Monitor Unit for requirements on Power Supply Monitoring, Watchdog Timer, FAILED State Output Circuits and Monitor Unit Reset.

3.6.3 CONFLICT MONITORING
The monitor shall sense up to 16 Channels for conflict (32 field outputs of Green and Yellow). The Green and Yellow are Logically ORed together. The associated cabinet output file assignment or operator selected output switches shall determine channel assignment.

3.6.3.1
All monitored field output voltages shall be measured as true RMS responsive (up to 3 KHz) to both positive and negative alternations of the sine wave and the full cycle. The calculated value shall be averaged over a minimum of 2 cycles. If digital means are used in calculating RMS, a minimum of 2 samples shall be taken per alternation.

3.6.3.2
Sensed conflicting field output voltages 25 VAC or greater for a duration of 500 ms or longer shall cause a FAILED state. Sensed conflicting field output voltages between 15 VAC or less OR any voltage having a duration of 200 ms or less shall NOT cause a FAILED states. Sensed conflicting field output voltages between 15 and 25 VAC and for durations between 200 and 500 ms may or may not cause a FAILED state.

3.6.3.3
The conflict monitoring circuitry shall be capable of detecting both a positive and negative half-wave failure under the foregoing conditions.

3.6.3.4
A FAILED state caused by sensing voltage conflicts shall be reset only by the Unit Reset.

3.6.3.5
Sixteen indicators shall be provided on the unit front panel to indicate if the channel output is sensed ON. The indicators shall remain ON in a latched state during a FAILED state unless unlatched by Unit Reset or a unit loss of power during said FAILED state.

3.6.4
Conflict Programming Card

3.6.4.1
A plug-in PCB Programming Card shall be provided in the monitor unit. The card shall plug into the unit through a slot in the unit front panel. The card shall contain 120 diodes (#1N4148 or equal). Each diode shall match 1 through 16 channels of possible conflict. The programming card shall be logically labeled and laid out for easy identification of the diodes by channel. With diodes in place all output channels being monitored shall be in conflict. When the diode (anode to numerical pins and cathode to alphabetical pins) has been removed the channels shall be defined as non-conflict.

3.6.4.2
A pad for 16 yellow inhibit jumpers shall be provided. Placement of the associated channel jumpers shall be provided. Placement of the associated channel jumper between the channel yellow pin the yellow inhibit common shall disable sensing the said channel yellow.

3.6.4.3
The programming card shall intermate with a PCB 28/56S Connector. The card shall be provided with card ejectors. The monitor unit shall provided a mechanically sound card and connector support including continuous card guides. When the programming card is resident in the unit, the card's front end shall be flushed with the unit's front panel.

3.6.4.4
Pins 16 and T shall be connected together on the programming card. Removal of the card shall be sensed as a conflicting FAILED state.

3.6.5
A front panel indicator labeled "CONFLICT" shall be provided. The indicator shall illuminate when there is a FAILED state caused by conflicting channels and go off only by Unit Reset Issuance.

3.6.6
The output relay contact for FAILED State shall be "CLOSED".

3.6.7
A second output circuit (STOPTIME controller input) shall be provided to sink a NPN Open Collector Transistor upon FAILED state. The transistor shall be rated to sink a minimum of 50 ma at up to 30 VDC. A blocking diode shall be provided on the transistor output to prevent it from souring power into the controller unit.

3.6.8
An internal SPST LOGIC toggle switch shall be provided on the Model 210 Monitor Unit to activate the WDT function. When the switch is ON the WDT Circuitry shall be active. The switch shall be mounted on the module PCB in a readily accessible location.

3.6.9
The Front Panel RESET Switch shall be tied to the External Test Reset Input Line (Pin Z). The External Line shall be optically isolated from internal circuitry.

CHAPTER 3 SECTION 7

MODEL 212 ITS CABINET MONITOR UNIT (CMU)

3.7.1 GENERAL

3.7.1.1

The CMU is the principle part of the ITS Cabinet Monitoring System. It is resident in the Power Distribution Assembly ITS (PDA ITS). The role of the CMU is to query various cabinet conditions and, if the application requires action, the CMU will transfer control from the Advance Transportation Controller Unit (ATC) to a safe control mode (Signalized Intersection or Ramp Metering). Some applications may not require any action, only data gathering and report back to the ATC.

3.7.1.2

The CMU is composed of a microprocessor, memory devices including non-volatile memory, communications circuitry to interface with Serial Buses #1 and #3, front panel indicators, front panel communication connector and a serial memory key device (DATAKEY). The Operating Program shall be resident in the Non-volatile memory. The DATAKEY shall possess the conditions and function selections of the Unit. A list of inclusive unit operational monitoring functions is as follows:

1. **Cabinet Power Supplies Monitor**
2. **Conflicting Channel Monitor**
3. **Serial Bus #1 & #3 Error**
4. **Message 62**
5. **Diagnostic Error**
6. **Multiple Channel Inputs**
7. **Lack of Signal Inputs**
8. **Yellow Clearance**
9. **Yellow plus Red Clearance**
10. **Police and PDA Flash Switch Monitor**
11. **Door Switches and Main Contactor Status**
12. **Circuit Breakers**
13. **Flasher Unit Output Status**

14. AC Line level sense

15. Field Output Monitor

3.7.1 FAILED STATE ACTION (FSA)

Only Unit Reset shall reset the CMU from a LATCHED FAILED STATE ACTION (LFSA). Only a Unit Reset or a CMU Power Fail shall reset a LATCHED RESETTABLE FAILED STATE ACTION (LFSA-R). A NONLATCHED FAILED STATE ACTION (NFSA) shall be reset if the fault conditions causing the NFSA have been removed. An NFSA shall last for the programmed Minimum Flash time at a minimum. Only one LFSA, LFSA-R or NFSA fault state shall be set at any time.

3.7.2 UNIT RESET

The CMU shall be reset from a FSA as a result of the Front Panel Reset Button or the EXTERNAL TEST RESET Input. This reset command shall be a one-time event such that a continuous reset command does not prevent the CMU from operating. The EXTERNAL TEST RESET Input shall be isolated from the AC+ RAW circuitry.

The EXTERNAL TEST RESET Input shall be True when the voltage is less than 8 VDC. The EXTERNAL TEST RESET Input shall be False when the voltage is greater than 16 VDC. A minimum True pulse width on the EXTERNAL TEST RESET Input of 100 milliseconds shall be required for a Unit Reset.

3.7.3 EXIT FROM FAILED STATE ACTION

Prior to the CMU transferring the Output Relay contacts from the Fault state to the No Fault state, a transition period of 500 milliseconds shall occur. During the transition period the Output Relay contacts shall be in the Fault state and the CMU shall set the Start-Up Flash Call bit in the Message 189 Frame to 1. At all other times the Start-Up Flash Call bit shall be set to 0.

3.7.4 MONITOR FUNCTIONS

3.7.4.1 CABINET POWER SUPPLY

The CMU shall sense the Cabinet +24 VDC and +12 VDC Power Supply sources to ± 5% accuracy. The CMU shall also sense the Cabinet +24 VDC state in each Output Assembly as reported by each AMU. Voltages equal to or greater than +22 VDC and +11 VDC respectively shall NOT cause a LFSA. Voltages at or less than +18 VDC and +9 VDC for 500ms or longer shall cause a LFSA. If the sensed voltage is less than +22 or +11 VDC for 200 ms or less, the CMU shall NOT cause a LFSA. All other timing or voltage conditions may or may not cause LFSA. A +24 VDC failure or +12 VDC failure during the programmed Minimum Flash Time or during a CMU Power Failure shall not cause a LFSA. The CMU shall report the value of the +24 VDC and +12 VDC power supply sources in the Message 189 Response Frame. There shall be programming in the DATAKEY to disable +12 VDC power supply monitoring.

3.7.4.2 CONFLICTING CHANNELS

For purpose of conflict determination, an active signal on either of the Green/Walk or Yellow inputs associated with any of the 32 channels shall be considered as that channel being active. The DATAKEY shall contain the permissive channel pair programming. When any conflicting channels are detected as concurrently active for less than 200 milliseconds the CMU shall not cause a LFSA. When any conflicting channels are detected as concurrently active for 500 milliseconds or more, the CMU shall cause a LFSA. When any conflicting channels are detected as concurrently active for more than 200 milliseconds but less than 500 milliseconds, the CMU may or may not cause a LFSA. The time interval between the beginning of the concurrently conflicting channels and the transfer to the LFSA shall not exceed 500 milliseconds.

3.7.4.3 SERIAL BUS ERROR

The CMU communicates with both Serial Bus (SB) #1 and #3. In SB #1 the CMU is a Secondary, polled by the ATC Primary. On SB #1, the CMU shall respond to the Serial Bus #1 Address defined in the DATAKEY. In SB #3 the CMU is the Primary, polling each AMU Secondary. See Chapter 3 Section 8 "AMU" for protocol.

3.7.4.3.1 SERIAL BUS #1 ERROR

The CMU shall cause a FSA when a Message 61 Frame has not been received from the ATC for greater than 1 second. If a CMU Power Fail resets the LFSA-R, the SB #1 timeout count shall be reset to 2 such that the next SB #1 timeout results in a LFSA-R.

A SB #1 timeout failure during the programmed Minimum Flash time or during a CMU Power Failure shall not cause a FSA. The SB #1 Timeout function shall be disabled if the SB #1 DISABLE input is at a True (Low) state.

The SB #1 DISABLE input shall be True when the voltage is less than 8 VDC. The SB #1 DISABLE input shall be False when the voltage is greater than 16 VDC. The SB #1 DISABLE input shall be isolated from the AC+ RAW circuitry.

3.7.4.3.2 SERIAL BUS #3 ERROR

The CMU shall cause a FSA when either Message 129 or 130 Frames have not been received from each AMU for greater than 300 milliseconds. If a CMU Power Fail resets the LFSA-R, the SB #3 timeout count shall be reset to 2 such that the next SB #3 timeout results in a LFSA-R. A SB #3 timeout failure during the programmed Minimum Flash time or during a CMU Power Failure shall not cause a FSA.

3.7.4.4 MESSAGE 62

If the "N" bit is set in a Message 62, the CMU shall react by causing a NFSA. The NSFA shall remain until the receipt of a Message 62 with the "N" bit cleared or until the CMU is reset by a Unit Reset or CMU Power Fail. The NSFA shall last for the programmed Minimum Flash time at a minimum. If the "L" bit is set in Message 62, the CMU shall react by causing a LFSA.

3.7.4.5 DIAGNOSTICS

3.7.4.5.1 DIAGNOSTIC ERROR

The CMU shall be provided with a resident series of self-check diagnostic capabilities. The CMU shall contain provisions to verify all memory elements on power-up. When a fault is detected, the LFSA-R shall be set and the DIAGNOSTIC indicator illuminated.

3.7.4.5.2 RAM DIAGNOSTIC

This test shall verify that all RAM elements are operating correctly at power-up or following a Unit Reset. Patterns shall be written to RAM. Each write shall be followed by a read to verify that it contains the written pattern.

3.7.4.5.3 NONVOLATILE DIAGNOSTIC

This test shall verify that the Nonvolatile Memory contains the proper program. The routine shall perform a check on the memory and make a comparison with a preprogrammed check value. This test shall be performed at power-up and at a minimum rate of 1024 bytes per second during operation.

3.7.4.5.4 DATAKEY DIAGNOSTIC

This test shall verify whether the DATAKEY contains valid data and that the data has not changed since the last write. The routine shall perform a check on each nonvolatile memory element at power-up and make a comparison with a preprogrammed check value. The DATAKEY not present shall cause a LFSA if the DOOR SWITCH FRONT input is sensed as not active (closed). A check sum not valid shall cause LFSA.

3.7.4.5.5 INTERNAL MPU MONITOR

The CMU shall monitor the operation of its microprocessor with an independent circuit. At a minimum, the monitoring circuit shall receive logic state transitions at least once every 50 milliseconds from the microprocessor. When the logic state transition is not received for 500 milliseconds the monitor circuit shall force a LFSA-R and illuminate the DIAGNOSTIC indicator.

3.7.4.6 MULTIPLE INPUT

The CMU shall be capable of monitoring for the presence of an active signal on two or more inputs of a channel. When the presence of an active signal on two or more inputs of a channel is detected for less than 200 milliseconds, the CMU shall not cause a LFSA. When the presence of an active signal on two or more inputs to a channel is detected for 450 milliseconds or more, the CMU shall cause a LFSA. When the presence of an active signal on two or more inputs to a channel is detected for more than 200 milliseconds but less than 450 milliseconds, the CMU may or may not cause a LFSA. Multiple Input monitoring shall be disabled when the MC COIL STATUS input is not active. There shall be programming in the DATAKEY to disable Multiple Indication monitoring on a color combination basis (G+Y, Y+R, G+R).

3.7.4.7 LACK OF SIGNAL INPUTS

The CMU shall detect the absence of any required signal voltage OR signal current (CS) on the inputs of a channel. For voltage purposes a required signal on the Green or Yellow or Red inputs associated with a channel shall be considered as that channel being active. When an absence of an active channel is detected for less than 700 milliseconds, the CMU shall not cause a LFSA. When an absence of an active channel is detected for 1000 milliseconds or more, the CMU shall cause a LFSA. When an absence of an active channel is detected for more than 700 milliseconds but less than 1000 milliseconds, the CMU may or may not cause a LFSA. Lack of Signal Input monitoring shall be disabled for all channels when the MC COIL STATUS input is not active. There shall be programming in the DATAKEY to disable Lack of Signal Input monitoring on a per channel basis. Lack of Signal Input monitoring shall also be disabled for any channel which has the DARK CHANNEL MAP bit set to "1" in the DATAKEY programming for the DARK CHANNEL MAP addressed by the DARK CHANNEL MAP SELECT bits in a Message 61. The monitor function is hardwired to 28 physical channels, thus Virtual Channels do not have CS monitoring capability. The CS monitor function shall be disabled for any physical channel that has an input remapped to a Virtual Channel.

3.7.4.8 YELLOW CLEARANCE

The CMU shall verify that the Yellow Change interval is at least 3.1 ±0.1 seconds. When the minimum Yellow Change interval is not satisfied, the CMU shall cause a LSFA. The CMU shall report a Skipped Yellow Clearance when the Yellow Change interval is less than 100 milliseconds. The CMU shall report a Short Yellow Clearance when the Yellow Change interval is less than 3.1 ± 0.1 seconds and greater than 100 milliseconds. Minimum Yellow Change interval monitoring shall be disabled when the MC COIL STATUS input is not active. There shall be programming in the DATAKEY to disable Minimum Yellow Change interval monitoring on a per channel basis.

3.7.4.9 YELLOW PLUS RED CLEARANCE

The CMU shall verify that the Yellow Change plus Red Clearance interval between the end of an active GREEN signal and the beginning of the next conflicting GREEN signal is at least 3.1 ± 0.1 seconds. When the minimum Yellow Change plus Red Clearance interval is not satisfied, the CMU shall cause a LSFA. Minimum Yellow Change plus Red Clearance monitoring shall be disabled when the MC COIL STATUS input is not active. There shall be programming in the DATAKEY to disable Minimum Yellow Change plus Red Clearance interval monitoring on a per channel basis.

3.7.4.10 LOCAL FLASH STATUS

The CMU shall monitor the LF STATUS input. When this signal is sensed as not active for greater than 500 milliseconds the CMU shall cause a NFSA. When this signal is sensed as not active for less than 200 milliseconds the CMU shall not cause a NFSA.

3.7.4.11 LOCAL FLASH STATUS RECOVERY

Recovery from Local Flash Status NFSA shall occur when this signal is sensed as active for greater than 500 milliseconds. When this signal is sensed as active for less than 200 milliseconds the CMU shall not cause recovery from Local Flash Status NFSA.

3.7.4.12 CIRCUIT BREAKER TRIP STATUS

The CMU shall monitor the CB TRIP STATUS input. When this signal is sensed as not active for greater than 500 milliseconds the CMU shall cause a LFSA. When this signal is sensed as not active for less than 200 milliseconds the CMU shall not cause a LFSA.

3.7.4.13 FLASHER UNIT OUTPUT FAILED

The CMU shall monitor the FLASHER 1-1, FLASHER 1-2, FLASHER 2-1, FLASHER 2-2 voltage states reported by each AMU. These inputs shall be considered active when the input voltage exceeds 89 Vrms. These inputs shall not be considered active when the input voltage is less than 70 Vrms. Signals between 89 Vrms and 70 Vrms may or may not be considered active. When a transition from the inactive state to the active state or a transition from the active state to the inactive state is absent for greater than 2500 milliseconds, the CMU shall set a status bit in the Type 182 frame. This alarm condition shall not cause a FSA. It should cause the appropriate response in the CU. This status is non-latching such that once a status bit has been set, the sensing of five valid transitions of the input shall clear the status bit.

3.7.4.14 CMU POWER FAILURE

The CMU shall monitor the AC+ RAW Input and the NRESET and POWERDOWN cabinet control inputs to determine a CMU Power Failure Response. The POWERDOWN signal in the low state indicates loss of AC+ RAW in the ATC. A CMU Power Failure shall be recognized when both the POWERDOWN and NRESET signals are active low for greater than 100 ms or the AC+ RAW voltage is less than 82 ± 2 Vrms.

3.7.4.15 AC+ RAW LEVEL SENSE

The CMU shall monitor the AC+ RAW input plus AMU RAWs. When the AC+ RAW voltage is less than 82 ±2 Vrms for greater than 650 ± 100 ms the CMU shall cause a NFSA. Once NFSA has been set, the POWERDOWN and NRESET signals shall not be monitored until the AC+ RAW voltage has exceeded 87 ±2 Vrms.

3.7.4.16 POWER INTERRUPT

The CMU shall disable monitoring of the +12VDC and +24VDC power supply inputs when either the POWERDOWN or NRESET input is low. When the POWERDOWN and NRESET signals are both low the CMU shall cause a NFSA.

3.7.4.17 POWER RECOVERY

When the POWERDOWN input is high and the NRESET signal goes from low to high the CMU shall begin timing the programmed Minimum Flash Interval. During the Minimum Flash Interval the CMU shall be in NFSA.

3.7.4.18 POWER UP

Following initial application of AC+ RAW voltage the CMU shall maintain a NFSA until the POWERDOWN input is high and the NRESET signal goes from low to high. The CMU shall then begin timing the programmed Minimum Flash Interval. During the Minimum Flash Interval the CMU shall be in NFSA.

3.7.4.19 MINIMUM FLASH INTERVAL

During the Minimum Flash Interval the CMU shall be in NFSA. The Minimum Flash Interval shall be programmed in the Serial memory key between the limits of 6 seconds to 16 seconds with an incremental adjustment of 1 second. The CMU shall not set a FSA during the Minimum Flash Interval.

3.7.5 FIELD OUTPUT CHECK

3.7.5.1 FIELD CHECK MODE

The CMU shall compare the active states of the field signals with the states reported by the CU in the Message 61 frame. When a mismatch is detected for less than 700 milliseconds the CMU shall not cause a LFSA. When a mismatch is detected for 1000 milliseconds or more, the CMU shall cause a LFSA. When a mismatch is detected for more than 700 milliseconds but less than 1000 milliseconds, the CMU may or may not cause a LFSA. Field Output Check monitoring shall be disabled when the MC COIL STATUS input is not active. There shall be a programming in the DATAKEY to disable Field Output Check monitoring on a field input basis.

3.7.5.2 FIELD CHECK STATUS

The CMU shall compare the active states of the field signals with the states reported by the ATC in the Message 61 frame. When a mismatch is detected while a Conflict, Lack of Signal, or Multiple fault is timing, Field Check Status shall be reported with the fault to indicate the faulty channel(s) and color(s). Field Output Check monitoring shall be disabled when the CB COIL STATUS input is not active. There shall be a programming in the DATAKEY to disable Field Output Check monitoring on a field input basis.

3.7.6 CMU TEMPERATURE

The CMU shall measure the temperature at the CMU and report this value in the Message 189 frame. Temperature accuracy shall be ± 6 degrees centigrade over the operating temperature range of the CMU.

3.7.6.1 INPUT SIGNALS

3.7.6.2 FIELD SIGNAL INPUTS

A Green or Yellow signal input shall be sensed active when it exceeds 25 Vrms and shall not be sensed active when it is less than 15 Vrms. A Green or Yellow signal between 15 and 25 Vrms may or may not be sensed active. There shall be a programming in the DATAKEY to disable the Yellow input for each physical channel. A Red signal input shall be sensed active when it exceeds 70 Vrms and shall not be sensed active when it is less than 50 Vrms. A Red signal between 50 and 70 Vrms may or may not be sensed active.

3.7.6.3 LOAD SWITCH CURRENT

A channel shall be sensed active when the load current exceeds 105% of the Channel Current Sense Threshold programmed for that channel in the DATAKEY. A channel shall not be sensed active when the load current is less than 95% of the Channel Current Sense Threshold programmed for that channel in the DATAKEY. A load current value between 95% and 105% of the Channel Current Sense Threshold may or may not be sensed active. This provides a hysterisis value of ± 5% of the Channel Current Sense Threshold.

3.7.6.4 PDA CONTROL SIGNAL INPUTS (status reported to ATC in Message 189)

3.7.6.4.1 LOCAL FLASH STATUS

This input shall be internally connected to the CMU Output Relay COM pin. This input shall be considered active when the input voltage exceeds 89 Vrms. This input shall not be considered active when the input voltage is less than 70 Vrms. Signals between 89 Vrms and 70 Vrms may or may not be considered active. Operation of the cabinet in AUTO mode shall place AC+ on this input. Operation of the cabinet in FLASH mode shall be open circuit on this input.

3.7.6.4.2 MAIN CONTACTOR COIL (MC) STATUS

The MC COIL STATUS input shall be connected to the AC+ RAW side of the MC coil. An active signal on this input indicates the Signal Bus should be powering the load switches. This input shall be considered active when the input voltage exceeds 89 Vrms. This input shall not be considered active when the input voltage is less than 70 Vrms. Signals between 89 Vrms and 70 Vrms may or may not be considered active.

3.7.6.4.3 MC SECONDARY STATUS

The MC SECONDARY STATUS input shall be connected to the output side of the MC. This input shall be considered active when the input voltage exceeds 89 Vrms. This input shall not be considered active when the input voltage is less than 70 Vrms. Signals between 89 Vrms and 70 Vrms may or may not be considered active.

FTR COIL DRIVE STATUS

The FTR COIL DRIVE STATUS input shall be connected to the FTR COIL DRIVE signal in the AC SIGNAL POWER BUS. This input shall be considered active when the input voltage exceeds 89 Vrms. This input shall not be considered active when the input voltage is

less than 70 Vrms. Signals between 89 Vrms and 70 Vrms may or may not be considered active.

3.7.6.4.4 CIRCUIT BREAKER (CB) TRIP STATUS

The CB TRIP STATUS input shall be connected to the Auxiliary Switch output of the circuit breaker unit. This input shall be considered active when the input voltage exceeds 89 Vrms. This input shall not be considered active when the input voltage is less than 70 Vrms. Signals between 89 Vrms and 70 Vrms may or may not be considered active.

3.7.6.4.5 FRONT/REAR DOOR SWITCH

The CMU shall monitor the DOOR SWITCH FRONT and DOOR SWITCH REAR inputs. These inputs shall be considered active (door open) when the input voltage exceeds 89 Vrms. These inputs shall not be considered active (door closed) when the input voltage is less than 70 Vrms. Signals between 89 Vrms and 70 Vrms may or may not be considered active.

3.7.6.4.6 MONITOR INTERLOCK

The MONITOR INTERLOCK input shall be connected to Logic Ground within the CMU.

3.7.7 POWER AND CIRCUIT REQUIREMENTS

3.7.7.1 AC+ RAW

The CMU shall be operational over the voltage range of 80 to 135 Vrms. It shall be capable of insertion and removal while AC power is applied to the cabinet. Surge current on AC+ RAW shall be less than 2 Amps peak.

3.7.7.1.1 +24VDC Power Supply

The CMU shall not use the Cabinet +24VDC Power Supply to run any of its internal circuitry. The +24VDC MONITOR and +12VDC MONITOR input circuits shall be optically isolated from the AC+ RAW circuitry. The maximum current into the +24VDC or +12VDC Monitor inputs over the voltage range of 0 to 30 VDC shall be less than 20 milliamps.

3.7.7.2 FAILED STATE OUTPUT CIRCUIT

The Output relay of the CMU shall have one set of isolated Form C contacts. These relay contacts shall be rated for a minimum of 3 amperes at 120 Vrms and 100,000 operations. Contact opening/closing time shall be 30 ms or less. The relay coil shall be energized in the No Fault state and de-energized in the FSA state.

3.7.8 FRONT PANEL DEVICES

3.7.8.1 INDICATORS

All indicators shall be LEDS. The following indicators shall be provided (Top to Bottom):

3.7.8.2 POWER

A POWER indicator shall illuminate to indicate AC+ RAW voltage is proper. It shall flash at a 2 Hz rate when the NRESET or POWERDOWN input is True. It shall remain off when the voltage is less than 80 ± 2 Vrms.

3.7.8.3 24VDC FAIL

A 24VDC FAIL indicator shall illuminate when the CMU is in FSA as a result of a 24VDC cabinet power supply fault.

3.7.8.4 12VDC FAIL

A 12VDC FAIL indicator shall illuminate when the CMU is in FSA as a result of a 12VDC cabinet power supply fault. The 12VDC FAIL indicator shall flash at a 0.5 Hz rate when the 12VDC monitor function is disabled.

3.7.8.5 CONFLICT

A CONFLICT indicator shall illuminate when the CMU is in FSA as a result of a Conflicting Channels fault.

3.7.8.6 LACK OF SIGNAL

A LACK OF SIGNAL indicator shall illuminate when the CMU is in FSA as a result of a Lack of Signal Inputs fault.

3.7.8.7 MULTIPLE

A MULTIPLE indicator shall illuminate when the CMU is in FSA as a result of a Multiple Inputs fault.

3.7.8.8 ATC / LOCAL FLASH

An ATC / LOCAL FLASH indicator shall illuminate when the CMU is in FSA as a result of a Message 62 command from the ATC, the LOCAL FLASH STATUS input sensed inactive, or CB TRIP STATUS active.

3.7.8.9 CLEARANCE

A CLEARANCE indicator shall illuminate when the CMU is in FSA as a result of a Yellow Clearance or Yellow Plus Red Clearance fault.

3.7.8.10 FIELD CHECK

A FIELD CHECK indicator shall illuminate when the CMU is in FSA as a result of a Field Output Check fault. The indicator shall flash at a 2Hz rate when the CMU is in FSA with Field Check Status as a result of Conflict, Lack of Signal, or Multiple fault.

3.7.8.11 SB #1 ERROR

A SB #1 ERROR indicator shall illuminate when the CMU is in FSA as a result of a Serial Bus #1 fault.

3.7.8.12 SB #3 ERROR

A SB #3 ERROR indicator shall illuminate when the CMU is in FSA as a result of a Serial Bus #3 fault.

3.7.8.13 DIAGNOSTIC

A DIAGNOSTIC indicator shall illuminate when the CMU is in FSA as a result of a Diagnostic fault.

3.7.8.14 SB #1 RX

A SB #1 RX indicator shall illuminate for 20 ± 5 milliseconds each time the CMU correctly receives a frame on Serial Bus #1.

3.7.8.15 SB #3 RX

A SB #3 RX indicator shall illuminate for 20 ± 5 milliseconds each time the CMU correctly receives a frame on Serial Bus #3.

3.7.9 SERIAL BUS #3 TERMINATIONS

The Serial Bus #3 RxDATA+ input shall be terminated on the CMU to the Serial Bus #3 RS-485 supply voltage through a 560 ohm resistor. The Serial Bus #3 RxDATA- input shall be terminated on the CMU to AC – RAW through a 560 ohm resistor. A 120 ohm resistor shall be connected on the CMU between RxDATA+ and Rx DATA-. The CMU Serial Bus #3 TxDATA drivers shall remain in the mark state with drivers enabled when the CMU is not transmitting a command frame.

3.7.10 TERMINAL PORT

An EIA-232-E Data Terminal Equipment (DTE) interface and connector shall be provided for interconnecting to a personal computer. Where differences occur between the EIA-232 Standard and this document, this document shall govern.

3.7.10.1 RECEIVE DATA (RxDATA)

The RxDATA input shall contain the serial data input to the CMU.

3.7.10.2 TRANSMIT DATA (TxDATA)

The TxDATA output shall contain the serial data output from the CMU.

3.7.10.3 SIGNAL GROUND

All signals shall be referenced to Signal Ground and shall be optically isolated from the CMU.

3.7.10.4 DATA LINK LAYER

Transmission shall be in asynchronous start/stop mode. The format shall be 8 bit data, 1 stop bit, even parity, and 9600 bits/second ± 2% at a minimum. The CMU shall be capable of full duplex operation. Flow control shall use XON/XOFF procedures.

3.7.11 MONITOR UNIT DATAKEY

The CMU shall have a Datakey^{tm} model KC4210 Keyceptacle^{tm} socket or equal mounted on the front panel containing a 16-kbit Datakey^{tm} P/N 611-0070-002 (RED) serial memory key or equal. The serial memory key shall be rated for –40 to +80 ^{o}C operation.

(Note: Datakey^{tm} and Keycepticle^{tm} are registered trademarks of Datakey, Inc.)

3.7.11.1 MONITOR UNIT SERIAL MEMORY KEY INTERFACE

The CMU shall not provide the capability to program the serial memory key. It shall be used as a read only device. The 16 bit Frame Check Sequence (FCS) procedure defined in clause 4.6.2 of ISO/IEC 3309 shall be used to verify the integrity of the read data. To generate the write FCS, the initial FCS content is set to 0xFFFF. After calculating bytes #1 through #510, the ones complement of the result shall be stored in bytes #511 and #512. To generate the read FCS, the initial FCS content is set to 0xFFFF. After calculating bytes #1 through #512, the FCS calculation shall result in a sum of 0x1D0F when data is read correctly. Failure to read the serial memory key correctly shall result in LFSA. Interface circuitry to the device shall utilize the LOFO switch on the serial memory key socket to ensure the device is removed and inserted with no power applied to the interface pins (i.e. dead socket).

3.7.11.2 SERIAL MEMORY KEY DATA

All bytes and bits marked as "reserved" shall be set to "0".

Byte #	Contents	Description
1	0x01	Serial Memory Key Version
2	Ch 1-9…1-2	Permissive Programming for channels 1-32: A bit set to "1" programs a channel pair to the permissive state. In the event the CMU has fewer than 32 channels, the bit positions corresponding to the nonexistent channels shall be 0. Default programming shall be 0.
3	Ch 1-17…1-10	
4	Ch 1-25…1-18	
5	Ch 2-3…1-26	
6	Ch 2-11…2-4	
7	Ch 2-19…2-12	
8	Ch 2-27…2-20	
9	Ch 3-6…2-28	
10	Ch 3-14…3-7	
11	Ch 3-22…3-15	
12	Ch 3-30…3-23	
13	Ch 4-10…3-31	
14	Ch 4-18…4-11	
15	Ch 4-26…4-19	
16	Ch 5-7…4-27	
17	Ch 5-15…5-8	
18	Ch 5-23…5-16	
19	Ch 5-31…5-24	
20	Ch 6-13…5-32	
21	Ch 6-21…6-14	
22	Ch 6-29…6-22	
23	Ch 7-12…6-30	
24	Ch 7-20…7-13	
25	Ch 7-28…7-21	
26	Ch 8-12…7-29	
27	Ch 8-20…8-13	
28	Ch 8-28…8-21	
29	Ch 9-13…8-29	
30	Ch 9-21…9-14	
31	Ch 9-29…9-22	
32	Ch 10-15…9-30	
33	Ch 10-23…10-16	
34	Ch 10-31…10-24	
35	Ch 11-18…10-32	
36	Ch 11-26…11-19	
37	Ch 12-14…11-27	
38	Ch 12-22…12-15	
39	Ch 12-30…12-23	
40	Ch 13-19…12-31	
41	Ch 13-27…13-20	
42	Ch 14-17…13-28	
43	Ch 14-25…14-18	

44	Ch 15-16…14-26	
45	Ch 15-24…15-17	
46	Ch 15-32…15-25	
47	Ch 16-24…16-17	
48	Ch 16-32…16-25	
49	Ch 17-25…17-18	
50	Ch 18-19…17-26	
51	Ch 18-27…18-20	
52	Ch 19-22…18-28	
53	Ch 19-30…19-23	
54	Ch 20-26…19-31	
55	Ch 21-23…20-27	
56	Ch 21-31…21-24	
57	Ch 22-29…21-32	
58	Ch 23-28…22-30	
59	Ch 24-28…23-29	
60	Ch 25-29…24-29	
61	Ch 26-31…25-30	
62	Ch 28-30…26-32	
63	Ch 31-32…28-31	
64	Ch 8:1	Lack of Signal Input Enable: A bit set to "1" enables the Lack of Signal Input monitoring function for that channel. This bit shall be set to "0" for any channel that has an input mapped to a virtual channel. In the event the CMU has fewer than 32 channels, the bit positions corresponding to the nonexistent channels shall be 0. Default programming shall be 1.
65	Ch 16:9	
66	Ch 24:17	
67	Ch 32:25	
68	Ch 8:1	Dark Channel Map #1 A bit set to "1" disables the Lack of Signal Input monitoring function for that channel. For channels that are set to 0, Lack of Signal Input Enable programming shall determine Lack of Signal Input operation. Default programming shall be 0.
69	Ch 16:9	
70	Ch 24:17	
71	Ch 32:25	
72	Ch 8:1	Dark Channel Map #2 A bit set to "1" disables the Lack of Signal Input monitoring function for that channel. For channels that are set to 0, Lack of Signal Input Enable programming shall determine Lack of Signal Input operation. Default programming shall be 0.
73	Ch 16:9	
74	Ch 24:17	
75	Ch 32:25	
76	Ch 8:1	Dark Channel Map #3 A bit set to "1" disables the Lack of Signal Input monitoring function for that channel. For channels that are set to 0, Lack of Signal Input Enable programming shall determine Lack of Signal Input operation. Default
77	Ch 16:9	

78	Ch 24:17	
79	Ch 32:25	
80	Ch 8:1	Dark Channel Map #4 A bit set to "1" disables the Lack of Signal Input monitoring function for that channel. For channels that are set to 0, Lack of Signal Input Enable programming shall determine Lack of Signal Input operation. Default programming shall be 0.
81	Ch 16:9	
82	Ch 24:17	
83	Ch 32:25	
84	Ch 8:1	GY Multiple Channel Enable: A bit set to "1" enables the Green / Yellow Multiple Channel monitoring function for that channel. This bit shall be set to "0" for any channel that has had a Green or Yellow input remapped to a virtual channel. In the event the CMU has fewer than 32 channels, the bit positions corresponding to the nonexistent channels shall be 0. Default programming shall be 1.
85	Ch 16:9	
86	Ch 24:17	
87	Ch 32:25	
88	Ch 8:1	YR Multiple Channel Enable: A bit set to "1" enables the Yellow / Red Multiple Channel monitoring function for that channel. This bit shall be set to "0" for any channel that has had a Yellow or Red input remapped to a virtual channel. In the event the CMU has fewer than 32 channels, the bit positions corresponding to the nonexistent channels shall be 0. Default programming shall be 1.
89	Ch 16:9	
90	Ch 24:17	
91	Ch 32:18	
92	Ch 8:1	GR Multiple Channel Enable: A bit set to "1" enables the Green / Red Multiple Channel monitoring function for that channel. This bit shall be set to "0" for any channel that has had a Green or Red input remapped to a virtual channel. In the event the CMU has fewer than 32 channels, the bit positions corresponding to the nonexistent channels shall be 0. Default programming shall be 1.
93	Ch 16:9	
94	Ch 24:17	
95	Ch 32:25	
96	Ch 8:1	Minimum Yellow Change Enable: A bit set to "1" enables the Minimum Yellow Change monitoring function for that channel. In the event the CMU has fewer than 32 channels, the bit positions corresponding to the nonexistent channels shall be 0. Default programming shall be 1.
97	Ch 16:9	
98	Ch 24:17	

99	Ch 32:18	
100	Ch 8:1	Minimum Yellow Change Plus Red Clearance Enable: A bit set to "1" enables the Minimum Yellow Change Plus Red monitoring function for that channel. In the event the CMU has fewer than 32 channels, the bit positions corresponding to the nonexistent channels shall be 0. Default programming shall be 1.
101	Ch 16:9	
102	Ch 24:17	
103	Ch 32:18	
104	Ch 8:1	Yellow Input Disable: A bit set to "1" forces the Yellow input to the Off state for that channel. In the event the CMU has fewer than 28 physical channels, the bit positions corresponding to the nonexistent channels shall be 0. Default programming shall be 0.
105	Ch 16:9	
106	Ch 24:17	
107	Ch 28:25	
108	Ch 8:1	Current Sense Enable: A bit set to "1" enables the Lack of Indication current monitoring function for that channel. This bit shall be set to "0" for any channel that has an input mapped to a virtual channel. In the event the CMU has fewer than 24 physical channels, the bit positions corresponding to the nonexistent channels shall be 0. Default programming shall be 1.
109	Ch 16:9	
110	Ch 24:17	
111	Ch 28:25	
112	Ch 4:1	Current Sense Full Scale Parameter These bits shall define the Full Scale (FS) parameter for the Current Sense circuit for each channel. Default programming shall be 0xFF (2 Amp). b1,b0 = channel n b3,b2 = channel n+1 b5,b4 = channel n+2 b7,b6 = channel n+3 00 = .25 Amps 01 = .33 Amps 10 = .50 Amps 11 = 1.0 Amps
113	Ch 8:5	
114	Ch 12:9	
115	Ch 16:13	
116	Ch 20:17	
117	Ch 24:21	
118	Ch 28:25	
119	Channel 1	Channel Current Sense Threshold The threshold value for channel current sense shall be programmed in percent (0 to 95) of full scale (FS). This value should be set in accordance with minimum accuracy tolerances defined in AMU section 3.8.5.1, AC RMS CURRENT SENSING. Default programming shall be 25 (25% of 1 Amp full scale = 250mA).
120	Channel 2	
121	Channel 3	
122	Channel 4	
123	Channel 5	
124	Channel 6	
125	Channel 7	

126	Channel 8	
127	Channel 9	
128	Channel 10	
129	Channel 11	
130	Channel 12	
131	Channel 13	
132	Channel 14	
133	Channel 15	
134	Channel 16	
135	Channel 17	
136	Channel 18	
137	Channel 19	
138	Channel 20	
139	Channel 21	
140	Channel 22	
141	Channel 23	
142	Channel 24	
143	Channel 25	
144	Channel 26	
145	Channel 27	
146	Channel 28	
147	Red Ch 8:1	Field Output Check Enable: A bit set to "1" enables the Field Output Check monitoring function for that input. This bit shall be set to "0" for any input that has been remapped to a virtual channel. In the event the CMU has fewer than 32 channels, the bit positions corresponding to the nonexistent inputs shall be 0. Default programming shall be 1.
148	Yellow Ch 8:1	
149	Green Ch 8:1	
150	Red Ch 16:9	
151	Yellow Ch 16:9	
152	Green Ch 16:9	
153	Red Ch 24:17	
154	Yellow Ch 24:17	
155	Green Ch 24:17	
156	Red Ch 32:25	
157	Yellow Ch 32:25	
158	Green Ch 32:25	
159	6-15 seconds	Minimum Flash Time Values of 0 thru 5 shall result in 6 seconds of minimum flash. Default programming shall be 6.
160	+12 VDC Enable	+12VDC Power Supply Monitor Enable Bit 0 set to 1 shall enable the +12VDC Power Supply monitor. Default programming shall be 0x01.
161	Ch 29 Red	Virtual Channel Assignment Channels that have not been assigned shall be set to 0. Default programming shall be 0. Bits 4:0 specify the physical channel number (1 to 28) Bits 6:5 specify the physical input 01 = Red 10 = Yellow
162	Ch 29 Yellow	
163	Ch 29 Green	

164	Ch 30 Red	
165	Ch 30 Yellow	
166	Ch 30 Green	
167	Ch 31 Red	
168	Ch 31 Yellow	
169	Ch 31 Green	
170	Ch 32 Red	
171	Ch 32 Yellow	
172	Ch 32 Green	
173	AMU Position 1	AMU Configuration The number of load switch positions in each output Assembly position shall be programmed in each byte. CMU channel numbers shall be assigned sequentially starting with AMU position #1. Default programming shall be 14,0,0,0. 0: Position not used 6: Six Pack Output Assembly 14: Fourteen Pack Output Assembly All other values are reserved.
174	AMU Position 2	
175	AMU Position 3	
176	AMU Position 4	
177:216	Ascii string	Monitor ID A packed 40 character ID shall be stored in ASCII format. Allowable characters are 020h through 07Eh. If less than 40 characters are used, the unused locations shall be set to 00h. Default programming shall be 00h.
217:256	Ascii string	User ID A packed 40 character ID shall be stored in ASCII format. Allowable characters are 020h through 07Eh. If less than 40 characters are used, the unused locations shall be set to 00h. Default programming shall be 00h.
257:510	0x00	Reserved for future use.
511	FCS lsb	16 bit Check Value FCS Polynomial calculation of bytes #1 through #510.
512	FCS msb	

3.7.13 SERIAL BUS #1 FRAMES

3.7.13.1 MESSAGE 61 COMMAND - LOAD SWITCH DRIVERS

The destination of this frame is the CMU. The Channel numbers in the Description column below refer to the channel numbers of the CMU. The ATC shall include a definition, via program entry, of the CMU Channel to ATC signal driver group utilization. The Dark Channel Map Select Bits shall select a preprogrammed mask in the CMU DATAKEY that disables Lack of Signal Input monitoring for the selected channels.

Byte #	Contents	Description
1	61	Frame Message
2	Channel 8:1 Red	Load Switch Set A bit set to 1 indicates the Load Switch output is set On.
3	Channel 16:9 Red	
4	Channel 28:17 Red	
5	Channel 8:1 Yel	
6	Channel 16:9 Yel	
7	Channel 28:17 Yel	
8	Channel 8:1 Grn	
9	Channel 16:9 Grn	
10	Channel 28:17 Grn	
11	Map Select	Dark Channel Map Select Bit 1 and bit 0 shall select one of four Dark Channel Maps programmed in the serial memory key which disables Lack of Signal Input monitoring for a selected channel. Bits 2 thru 7 are reserved. 00 = Mask #1 01 = Mask #2 10 = Mask #3 11 = Mask #4

3.7.13.2 Message 189 RESPONSE – CMU STATUS

If the CMU is in FSA (byte #2, Fault Type not equal to 0), then all bytes of the information field of this frame except byte #31 Control Status shall contain an exact image of the signals that were applied to the CMU at the point in time of the detection of the failure. Byte #31, Control Status shall contain an exact image of the signals currently applied to the CMU. If a channel block is not used (AMU not present) the Channel Fault Status bits, Channel Input Status bits, and Channel Input Voltage values bits for that block shall be set to 0.

Byte #	Contents	Description
1	189	Frame Type
2	Fault Type	Enumerated fault code 00 = No Fault 01 = CMU/AMU +24VDC 02 = CMU +12VDC 03 = Conflict 04 = Serial Bus #1 05 = Serial Bus #3 06 = CU LFSA Flash (Type 62) 07 = CU NFSA Flash (Type 62) 08 = Diagnostic 09 = Multiple 10 = Lack of Signal Input 11 = Short Yellow Clearance 12 = Skipped Yellow Clearance 13 = Yellow + Red Clearance 14 = Field Output Check 15 = Serial Memory Key absent 16 = Serial Memory Key FCS error 17 = Serial Memory Key Data error 18 = Local Flash 19 = CB Trip 20 = CMU/AMU AC+ Main Fail 21 = nReset Active 22:127 = Reserved 128:255 = Spare
3	Channel Fault Status 8:1	Channel Fault Status Channel Fault Status bits shall be set to 1 for channels that were detected in fault for fault types 03, 09, 10, 11, 12, 13, and 14. For fault type 01, 05, and 20 a bit shall be set in Channel Fault Status 8:1 for each enabled AMU that failed. Bit 0 shall be set if the CMU detected a failure: b0 = CMU b1 = AMU #1 b2 = AMU #2 b3 = AMU #3 b4 = AMU #4 For all other fault types the Channel Fault Status bits shall be set to 0.
4	Channel Fault Status 16:9	
5	Channel Fault Status 24:17	
6	Channel Fault Status 32:25	

7	Channel Red Status 8:1	Channel Color Status Channel Color Status bits shall be set to 1 for channels that are sensed active. For channel inputs that have been remapped to a virtual channel (28-32), the Channel Fault Status bits shall be set to 0. For virtual channel (28-32) inputs that have not been assigned to a physical output, the Channel Fault Status bits shall be set to 0.
8	Channel Red Status 16:9	
9	Channel Red Status 24:17	
10	Channel Red Status 32:25	
11	Channel Yellow Status 8:1	
12	Channel Yellow Status 16:9	
13	Channel Yellow Status 24:17	
14	Channel Yellow Status 32:25	
15	Channel Green Status 8:1	
16	Channel Green Status 16:9	
17	Channel Green Status 24:17	
18	Channel Green Status 32:25	
19	Channel Red Status 8:1	Field Check Status Field Check Status bits shall be set to 1 for channels that are sensed with field check status. For channel inputs that have been remapped to a virtual channel (28-32), the Field Check Status bits shall be set to 0. For virtual channel (28-32) inputs that have not been assigned to a physical output, the Field Check Status bits shall be set to 0.
20	Channel Red Status 16:9	
21	Channel Red Status 24:17	
22	Channel Red Status 32:25	
23	Channel Yellow Status 8:1	
24	Channel Yellow Status 16:9	
25	Channel Yellow Status 24:17	
26	Channel Yellow Status 32:25	
27	Channel Green Status 8:1	
28	Channel Green Status 16:9	
29	Channel Green Status 24:17	
30	Channel Green Status 32:25	
31	Control Status #1	Control Status #1 b7 = Start-up Call (1=Exit from Flash) b6 = Flasher Output Fail (1 = Fail) b5 = Rear Door (1=Open) b4 = Front Door (1=Open) b3 = SB Coil (1=Active) b2 = SB Secondary (1=Active) b1 = FTR Coil Drive (1= Active) b0 = Output Relay Transfer (1=Fault)
32	Control Status #2	Control Status #2 b7 = Reserved b6 = Reserved b5 = Reserved b4 = Reserved b3 = Reserved b2 = Reserved b1 = Reserved b0 = Reserved
33	AC+ RAW Voltage	CMU AC+ RAW Voltage

34	Assembly #1 AC+ RAW	Assembly AC+ RAW Voltage
35	Assembly #2 AC+ RAW	
36	Assembly #3 AC+ RAW	
37	Assembly #4 AC+ RAW	
38	Channel 1 Red Voltage	Channel Input Voltages The Channel input voltages shall be the most recent values reported from the AMUs. For channel inputs that have been remapped to a virtual channel (29-32), the Channel Voltage value shall be set to 0. For virtual channel (29-32) inputs that have not been assigned to a physical output, the Channel Voltage value shall be set to 0.
39	Channel 2 Red Voltage	
40	Channel 3 Red Voltage	
41	Channel 4 Red Voltage	
42	Channel 5 Red Voltage	
43	Channel 6 Red Voltage	
44	Channel 7 Red Voltage	
45	Channel 8 Red Voltage	
46	Channel 9 Red Voltage	
47	Channel 10 Red Voltage	
48	Channel 11 Red Voltage	
49	Channel 12 Red Voltage	
50	Channel 13 Red Voltage	
51	Channel 14 Red Voltage	
52	Channel 15 Red Voltage	
53	Channel 16 Red Voltage	
54	Channel 17 Red Voltage	
55	Channel 18 Red Voltage	
56	Channel 19 Red Voltage	
57	Channel 20 Red Voltage	
58	Channel 21 Red Voltage	
59	Channel 22 Red Voltage	
60	Channel 23 Red Voltage	
61	Channel 24 Red Voltage	
62	Channel 25 Red Voltage	
63	Channel 26 Red Voltage	
64	Channel 27 Red Voltage	
65	Channel 28 Red Voltage	
66	Channel 29 Red Voltage	
67	Channel 30 Red Voltage	
68	Channel 31 Red Voltage	
69	Channel 32 Red Voltage	
70	Channel 1 Yellow Voltage	
71	Channel 2 Yellow Voltage	
72	Channel 3 Yellow Voltage	
73	Channel 4 Yellow Voltage	
74	Channel 5 Yellow Voltage	
75	Channel 6 Yellow Voltage	
76	Channel 7 Yellow Voltage	
77	Channel 8 Yellow Voltage	
78	Channel 9 Yellow Voltage	
79	Channel 10 Yellow Voltage	

80	**Channel 11 Yellow Voltage**	
81	**Channel 12 Yellow Voltage**	
82	**Channel 13 Yellow Voltage**	
83	**Channel 14 Yellow Voltage**	
84	**Channel 15 Yellow Voltage**	
85	**Channel 16 Yellow Voltage**	
86	**Channel 17 Yellow Voltage**	
87	**Channel 18 Yellow Voltage**	
88	**Channel 19 Yellow Voltage**	
89	**Channel 20 Yellow Voltage**	
90	**Channel 21 Yellow Voltage**	
91	**Channel 22 Yellow Voltage**	
92	**Channel 23 Yellow Voltage**	
93	**Channel 24 Yellow Voltage**	
94	**Channel 25 Yellow Voltage**	
95	**Channel 26 Yellow Voltage**	
96	**Channel 27 Yellow Voltage**	
97	**Channel 28 Yellow Voltage**	
98	**Channel 29 Yellow Voltage**	
99	**Channel 30 Yellow Voltage**	
100	**Channel 31 Yellow Voltage**	
101	**Channel 32 Yellow Voltage**	
102	**Channel 1 Green Voltage**	
103	**Channel 2 Green Voltage**	
104	**Channel 3 Green Voltage**	
105	**Channel 4 Green Voltage**	
106	**Channel 5 Green Voltage**	
107	**Channel 6 Green Voltage**	
108	**Channel 7 Green Voltage**	
109	**Channel 8 Green Voltage**	
110	**Channel 9 Green Voltage**	
111	**Channel 10 Green Voltage**	
112	**Channel 11 Green Voltage**	
113	**Channel 12 Green Voltage**	
114	**Channel 13 Green Voltage**	
115	**Channel 14 Green Voltage**	
116	**Channel 15 Green Voltage**	
117	**Channel 16 Green Voltage**	
118	**Channel 17 Green Voltage**	
119	**Channel 18 Green Voltage**	
120	**Channel 19 Green Voltage**	
121	**Channel 20 Green Voltage**	
122	**Channel 21 Green Voltage**	
123	**Channel 22 Green Voltage**	
124	**Channel 23 Green Voltage**	
125	**Channel 24 Green Voltage**	

126	Channel 25 Green Voltage	
127	Channel 26 Green Voltage	
128	Channel 27 Green Voltage	
129	Channel 28 Green Voltage	
130	Channel 29 Green Voltage	
131	Channel 30 Green Voltage	
132	Channel 31 Green Voltage	
133	Channel 32 Green Voltage	
134	Channel 1	Scaled Channel Load Current The value reported shall be the measured current in Amps times 256 divided by the Full Scale (FS) parameter. For 1 primary turn, FS=1 (range is 0 to 1 Arms) For 2 primary turns, FS=0.5 (range is 0 to 0.5 Arms) For 3 primary turns, FS= 0.33 (range is 0 to 0.33 Arms) For 4 primary turns, FS=0.25 (range is 0 to 0.25 Arms)
135	Channel 2	
136	Channel 3	
137	Channel 4	
138	Channel 5	
139	Channel 6	
140	Channel 7	
141	Channel 8	
142	Channel 9	
143	Channel 10	
144	Channel 11	
145	Channel 12	
146	Channel 13	
147	Channel 14	
148	Channel 15	
149	Channel 16	
150	Channel 17	
151	Channel 18	
152	Channel 19	
153	Channel 20	
154	Channel 21	
155	Channel 22	
156	Channel 23	
157	Channel 24	
158	Channel 25	
159	Channel 26	
160	Channel 27	
161	Channel 28	
162	BCD Seconds	CMU Time and Date
163	BCD Minutes	
164	BCD Hours (0:23)	
165	BCD Date	
166	BCD Month	
167	BCD Year	
168	Voltage * 4	24VDC Supply Voltage
169	Voltage * 8	12VDC Supply Voltage
170	^{o}C + 40	CMU Temperature (Centigrade)

171	Channel 8:1	Channel Current Sense Status Status bits shall be set to 1 for channels that are sensed active. Status bits shall be set to 0 for channels that have the Current Sense monitor function disabled.
172	Channel 16:9	
173	Channel 24:17	
174	Channel 28:25	
175	Assembly 2:1	Output Assembly Flasher Status (1=Fail) b0 = Assembly #1 (#3) FL1-1 b1 = Assembly #1 (#3) FL1-2 b2 = Assembly #1 (#3) FL2-1 b3 = Assembly #1 (#3) FL2-2 b4 = Assembly #2 (#4) FL1-1 b5 = Assembly #2 (#4) FL1-2 b6 = Assembly #2 (#4) FL2-1 b7 = Assembly #2 (#4) FL2-2
176	Assembly 4:3	
177		Reserved
178		Reserved

3.7.13.3 MESSAGE 62 COMMAND – SET FSA

Byte #	Contents	Description
1	62	Frame Message
2	FSA mode	Set Failed State Action b0 = Set LFSA (L) b1 = Set NFSA (N) b2:7 = reserved

3.7.13.4 MESSAGE 190 RESPONSE – HAVE SET FSA

Byte #	Contents	Description
1	190	Frame Message

3.7.13.5 MESSAGE 65 COMMAND – GET CMU CONFIGURATION

During initialization and once per second the ATC shall request the DATAKEY programming using this message and validate that the CMU Permissive Program settings are equal or less permissive than the ATC programming. If the programming of the CMU is not proper, the ATC shall issue a Message 62 frame with the L bit set causing a LFSA in the CMU.

Byte #	Contents	Description
1	65	Frame Message

3.7.13.6 MESSAGE 193 RESPONSE – CMU CONFIGURATION

Byte #	Contents	Description
1	193	Frame Message
2:513	Bytes #1 thru #512	DATAKEY Contents

CHAPTER 3 SECTION 8

MODEL 214 ITS AUXILIARY MONITOR UNIT (AMU)

3.8.1 GENERAL

The AMU shall reside in each of the cabinet output assemblies. the AMU shall interface with the Cabinet Monitor Unit (CMU) via Serial Bus #3. An AMU shall operate in a 14 channel mode (14-pack) or a 6 channel mode (6-pack) depending on the address select inputs. The sensed voltages and currents shall be reported to the CMU via the Serial Bus #3 response frames 129 or 130.

3.8.1.1 AMU ADDRESSING

The Address Select Input Pins ADDRESS 0, ADDRESS 1, and ADDRESS 2, define the Serial Bus #3 address of the AMU and the number of channels reported. The pins are left open for a logical False, and are connected to ADDRESS COMMON for a Logical True. If a 14-Pack Assembly is used, it shall be in Position 1 and 2. Position 3 is then either a 14-Pack or a 6-Pack Assembly. The 6-Pack Output Assembly shall have ADDRESS 2 permanently connected to ADDRESS COMMON on the assembly.

Mode / Position	ADDRESS 2	ADDRESS 1	ADDRESS 0	SB #3 Address
14 Ch / 1 and 2	False	False	True	0x01
14 Ch / 3 and 4	False	True	True	0x03
6 Ch / 1	True	False	True	0x05
6 Ch / 2	True	True	False	0x06
6 Ch / 3	True	True	True	0x07
6 Ch / 4	True	False	False	0x04

3.8.2 AC VOLTAGE SENSING

All AC RMS voltage measurements shall be made over a RMS period of 33.3 milliseconds (two AC Line cycles). All AC signals shall be sampled at a minimum of 1920 samples per second. A True RMS voltage measurement shall be made regardless of phase or wave-shape, including both positive and negative half-wave sinusoids, over the voltage range of 0 to 135 Vrms. AC voltage measurements shall be accurate to ±2 Vrms.

3.8.3 FIELD SIGNAL SENSING

Three inputs shall be provided for each of channel (Switch Pack) to permit the monitoring of voltages at the Green, Yellow, and Red signal field terminals. The AMU shall be designed so that unused Green, Yellow, or Red signal inputs are not sensed as active signals. The AMU shall sense an input at less than 15 Vrms when connected to AC Line through 1500 picofarads (pf).

3.8.4 AC LINE SENSING

The AMU shall include the capability of monitoring the AC Line Voltage applied to its AC+ RAW Input.

3.8.5 FLASHER UNIT INPUT SENSING

Four inputs shall be provided for sensing of voltages at the FLASHER Unit #1-1, FLASHER Unit #1-2, FLASHER Unit #2-1 and FLASHER Units #2-2 signal input terminals of the Output Assembly.

3.8.6 +24VDC SENSING

The AMU shall sense the state of the +24VDC Cabinet Power Supply Input. Voltages at or less than +18 VDC shall be considered LOW. The +24VDC voltage section shall be electrically isolated from the AC- Raw referenced circuitry.

3.8.7 CURRENT SENSING

3.8.7.1 AC RMS CURRENT SENSING

All AC RMS current measurements shall be made over a period of two AC Line Cycles (33.3 milliseconds). A True RMS current measurement shall be made regardless of phase or wave-shape, including both positive and negative half wave sinusoids. AC current measurements shall be accurate to ± 35%.

3.8.7.2 SWITCH PACK CURRENT SENSING

The AMU shall sense the total current of each switch pack. The input impedance of the COIL+ input with respect to the COIL- input shall be between 50 and 1000 ohms. Full scale current is set by the number of primary turns through the transformer and shall be a maximum of four turns. Unless specified otherwise, one turn shall be provided.

3.8.7.3 CURRENT TRANSFORMER PARAMETERS

The switch pack current sensing transformers shall meet the following requirements:

Linearity	**XX% from 10mA to 1A (single primary turn)**
Accuracy	**+/-25% (50 ohms < Rin < 1000 ohms)**
Secondary Turns	**1000**
Primary Current	**10 Amp maximum**
Minimum hole size	**0.25 inch diameter**
Insulation Resistance	**100 Mohms at 500 Vdc**

3.8.8 DIAGNOSTICS

The AMU shall be provided with a resident series of self-check diagnostic capabilities. At a minimum, the AMU shall contain provisions to verify all memory at Power-Up and Reset. When an error is detected, the AMU shall illuminate the ERROR Indicator and disable the Serial Bus #3 Port.

3.8.8.1 RAM DIAGNOSTIC

This test shall verify that all RAM elements are operating correctly. Patterns shall be written to RAM. Each Write shall be followed by a Read to verify that it contains the written pattern.

3.8.8.2 NONVOLATILE MEMORY DIAGNOSTIC

This test shall verify that the nonvolatile memory contain the proper program. The routine shall perform a check on memory and make a comparison with a preprogrammed check value. This test shall be performed at Power-Up, Reset and at a minimum rate of 1024 bytes per second during operation.

3.8.8.3 INTERNAL MPU MONITOR

The AMU shall monitor the operation of its microprocessor. At a minimum, the monitoring circuit shall be triggered at least every 100 milliseconds. The microprocessor shall be Reset and the ERROR Indicator illuminated if the monitoring circuit has not been triggered for a maximum of 1000 milliseconds.

3.8.9 POWER REQUIREMENTS

The AMU shall generate its own power supply voltage from the AC+ RAW Input using no more than 5 Watts. It shall be capable of insertion and removal while AC power is applied to the cabinet. Surge current on AC+ RAW Input shall be less than 2 Amps peak. The AMU shall be operational over the voltage range of 80 to 135 Vrms. The AMU shall be fully functional within 500 milliseconds following AC+ RAW Voltage exceeding 80 Vrms or Reset. During the loss of AC+ RAW Voltage for 700 milliseconds or less the AMU shall continue to operate.

3.8.10 FRONT PANEL DEVICES

3.8.10.1 AC POWER INDICATOR shall be provided. The indicator shall be illuminated when the AC+ RAW Input is 80 +/- 2Vrms or greater.

3.8.10.2 SERIAL BUS #3 INDICATOR shall be provided. The indicator shall pulse ON for 20 ms each time the AMU correctly receives a frame with its address on the Bus #3 Input.

3.8.10.3 ERROR INDICATOR The indicator shall be ON when an internal diagnostic or MPU error is detected.

3.8.10.4 RESET BUTTON A recessed RESET switch shall be provided which applies a

direct reset to the microprocessor device on the AMU. All voltage and current data shall be initialized to 0 following Reset. The access hole shall be 0.25 inches in diameter.

3.8.11 SERIAL BUS #3 PROFILE

3.8.11.1 DATA LINK LAYER

The data link layer protocol is based on a subset of HDLC as defined by ISO/IEC 3309. Transmission shall be in start/stop mode with basic transparency defined by clause 4.5.2.2 of ISO/IEC 3309 applied. The format shall be 8 bit data, 1 stop bit, no parity, and 153,600 bits per second ±2%. Only Asynchronous half-duplex operation shall be permitted. Each frame shall consist of the following fields:

1) **Flag byte = 0x7E**
2) **Address byte = 0x01 through 0x07**
3) **Control byte = 0x13 (U Format)**
4) **Information field = defined below in Section 3.8.12**
5) **Frame Check Sequence = 16 bit FCS procedure defined in clause 4.6.2 of ISO/IEC 3309.**
6) **Flag byte = 0x7E**

3.8.11.2 PROCEDURES

Frames transmitted by the CMU shall be referred to as command frames and frames transmitted by the AMU shall be referred to as response frames. Command frames shall be transmitted only to those AMUs that are present, as determined by the programming entries made in the CMU. Response frames shall only be transmitted as a result of correctly receiving a command frame. The first eight bits in each information field shall contain the frame Type number. There shall be a maximum of 64 different command frame types and 64 different response frame types. Additionally, there shall be 64 different command frame types reserved for special application use and 64 different response frame types reserved (Reserved bits shall always be set to zero by the transmitting station.) for special application use, as outlined below.

Frame Types	Function
1-63	Command frame defined by this specification
0, 64-127	Command frame reserved
128-191	Response frame defined by this specification
192-255	Response frame reserved

3.8.11.3 SERVICE TIME

The AMU shall begin its response to command frames from the CMU within a designated period of time following the correct reception of a complete command frame including the closing flag. This period shall be known as the Service Time and shall have a maximum value of 500 microseconds. The AMU TxData link output shall be in its high impedance state outside of the interval defined by the Service Time plus Response Time.

3.8.11.4 RESPONSE TIME

The AMU shall complete its transmission of the response frame including the closing flag within a designated time known as the Response Time, depending on the number of bytes transmitted in the response frame. The AMU TxData link output shall be in its high impedance state a maximum of 200 microseconds following the transmission of the closing flag. The Response Time period shall have a maximum value of (1.2)*(# of bytes in information field + 6)*(10/153600). Note that due to the transparency mechanism, any occurrence of the flag byte (0x7E) or control escape byte (0x7D) in the information field adds a second byte to the count. Thus the number of bytes in the information field could be doubled if all characters are 0x7E or 0x7D.

3.8.11.5 DEAD TIME

Following the transmission of each command frame, there shall be a Dead Time during which the CMU does not transmit. This Dead Time shall be a minimum of the Service Time plus the Response Time.

3.8.12 MESSAGE FRAMES

3.8.12.1 MESSAGE 1 COMMAND FRAME

This frame shall be transmitted from the CMU to each AMU-6 at least once every RMS period. Its purpose is to request the status from an AMU-6. Polling the AMU-6 more often than the RMS period may result in the same response frame being repeated.

Byte #	Contents	Description
1	01	Frame Type

3.8.12.2 MESSAGE 129 RESPONSE FRAME

This AMU-6 Response Frame shall be transmitted only if a CMU Message 1 Command Frame has been correctly received. The AMU-6 shall report the data for the most recent RMS period calculated when the Message 1 Command is received. The Message 1 command frame polling rate shall not affect the accuracy or RMS period of the data.

Byte #	Contents	Description
1	129	Frame Type
2	AMU Status	6 Pack AMU Status b0 = set to 1 if +24VDC MONITOR input is Low b1:4 = reserved b5 = set if AMU has reset since last poll b6 = set if last RMS period data was not transmitted b7 = diagnostic failure

3	0-135	AC+ RAW voltage
4	Channel 1 Red	Channel RMS Voltages
5	Channel 2 Red	
6	Channel 3 Red	
7	Channel 4 Red	
8	Channel 5 Red	
9	Channel 6 Red	
10	Channel 1Yellow	
11	Channel 2 Yellow	
12	Channel 3 Yellow	
13	Channel 4 Yellow	
14	Channel 5 Yellow	
15	Channel 6 Yellow	
16	Channel 1 Green	
17	Channel 2 Green	
18	Channel 3 Green	
19	Channel 4 Green	
20	Channel 5 Green	
21	Channel 6 Green	
22	Flasher #1-1	Flasher RMS Voltages
23	Flasher #1-2	
24	Flasher #2-1	
25	Flasher #2-2	
26	Channel 1	Channel Load Current The current value reported shall be the measured current in Amps times 255 divided by the Full Scale (FS) parameter. For 1 primary turn, FS =1.0 (range is 0 to 1.0A) For 2 primary turns, FS =0.5 (range is 0 to 0.5A) For 3 primary turns, FS =0.33 (range is 0 to 0.33A) For 4 primary turns, FS =0.25 (range is 0 to 0.25A)
27	Channel 2	
28	Channel 3	
29	Channel 4	
30	Channel 5	
31	Channel 6	
32	0	Reserved
33	0	Reserved

3.8.12.3 MESSAGE 2 COMMAND FRAME

This frame shall be transmitted from the CMU to each AMU-14 at least once every RMS period. Its purpose is to request the status from a AMU-14. Polling the AMU-14 more often than the RMS period may result in the same response frame being repeated.

Byte #	Contents	Description
1	02	Frame Type

3.8.12.4 MESSAGE 130 RESPONSE FRAME

This AMU-14 Response Frame shall be transmitted only if a CMU Message 2 Command Frame has been correctly received. The AMU-14 shall report the data for the most recent RMS period calculated when the Message 2 command is received. The Message 2 command frame polling rate shall not affect the accuracy or RMS period of the data.

Byte #	Contents	Description
1	130	Frame Type
2	AMU Status	14 Pack AMU Status b0 = set to 1 if +24VDC MONITOR input is Low b1:4 = reserved b5 = set if AMU has reset since last poll b6 = set if last RMS period data was not transmitted b7 = diagnostic failure
3	0-135	AC+ RAW voltage
4	Channel 1 Red	Channel RMS Voltages
5	Channel 2 Red	
6	Channel 3 Red	
7	Channel 4 Red	
8	Channel 5 Red	
9	Channel 6 Red	
10	Channel 7 Red	
11	Channel 8 Red	
12	Channel 9 Red	
13	Channel 10 Red	
14	Channel 11 Red	
15	Channel 12 Red	
16	Channel 13 Red	
17	Channel 14 Red	
18	Channel 1Yellow	
19	Channel 2 Yellow	
20	Channel 3 Yellow	
21	Channel 4 Yellow	
22	Channel 5 Yellow	
23	Channel 6 Yellow	
24	Channel 7Yellow	
25	Channel 8 Yellow	
26	Channel 9 Yellow	
27	Channel 10 Yellow	
28	Channel 11 Yellow	
29	Channel 12 Yellow	

30	Channel 13 Yellow	
31	Channel 14 Yellow	
32	Channel 1 Green	
33	Channel 2 Green	
34	Channel 3 Green	
35	Channel 4 Green	
36	Channel 5 Green	
37	Channel 6 Green	
38	Channel 7 Green	
39	Channel 8 Green	
40	Channel 9 Green	
41	Channel 10 Green	
42	Channel 11 Green	
43	Channel 12 Green	
44	Channel 13 Green	
45	Channel 14 Green	
46	Flasher #1-1	Flasher RMS Voltages
47	Flasher #1-2	
48	Flasher #2-1	
49	Flasher #2-2	
50	Channel 1	Channel Load Current The current value reported shall be the measured current in Amps times 255 divided by the Full Scale (FS) parameter. For 1 primary turn, FS =1.0 (range is 0 to 1A) For 2 primary turns, FS =0.5 (range is 0 to 0.5A) For 3 primary turns, FS =0.33 (range is 0 to 0.33A) For 4 primary turns, FS =0.25 (range is 0 to 0.25A)
51	Channel 2	
52	Channel 3	
53	Channel 4	
54	Channel 5	
55	Channel 6	

56	Channel 7	
57	Channel 8	
58	Channel 9	
59	Channel 10	
60	Channel 11	
61	Channel 12	
62		
63	Channel 13	
64	Channel 14	
65	0	Reserved
66	0	Reserved

3.8.12.5 MESSAGE 128 RESPONSE FRAME

This frame shall be transmitted from the AMU to the CMU as a Negative Acknowledge response frame if the AMU correctly receives a command frame with an invalid parameter.

Byte #	Contents	Description
1	128	Frame Negative Acknowledge
2	Status	AMU SB #3 Error b0 = set to 1 if invalid frame received b1:7 = reserved

CHAPTER 3 SECTION 9

MODEL 216-12 & 216-24 ITS POWER SUPPLY UNITS

3.9.1
The unit chassis shall be vented. The power supply cage and transformers shall be securely braced to prevent damage in transit. When resident in the PDA ITS, the units shall be held firmly in place by its stud screws and wing nut.

3.9.2
Two units, 216-12 and 216-24 shall provide +12 and +24 VDC to the cabinet assemblies. They shall be of ferro-resonant design. They shall have no active components and conform to the following requirements:

3.9.2.1
Line and load regulation shall meet the two power supply ranges for +24 VDC (23.0 to 26 VDC) and +12 VDC (11.65 to 13.35). This includes ripple noise; from 90 to 135 VAC at 60 Hz., plus an additional 1.6% for each additional 1.0% frequency change; and current range from 1 to 5 Amperes with a maximum temperature rise of 30 °C above ambient.

3.9.2.2
Design Voltage +24 ± 0.5 VDC and +12 VDC ± 0.5 VDC at full load, 30 °C, 115 VAC incoming after a 30-minute warm-up period.

3.9.2.3 Full Load Current 5 AMPS each for +24 VDC and +12 VDC, minimum.
3.9.2.4 Ripple Noise - 2 volts peak-to-peak and 500 millivolts RMS at full load.
3.9.2.5 Line Voltage - 90 to 135 VAC.
3.9.2.6 Efficiency - 70% minimum.
3.9.2.7 Circuit capacitors shall be rated for 40 volts minimum.

3.9.3
The front panel shall include AC and DC fuses, power ON light and test points for monitoring the output voltages. The unit including terminals shall be protected to prevent accidental contact with energized parts.

CHAPTER 3 SECTION 10
MODEL 218 ITS SERIAL INTERFACE UNIT (SIU)

3.10.1 GENERAL

3.10.1.1
The SIU functions as the ITS cabinet interface between the ATC controller unit and the cabinet Input / Output Assemblies providing communications and control.

3.10.1.2
The SIU shall be capable of communicating with Cabinet Serial Buses #1 & #2, the Input Assembly INBUS and the DB9 Connector for external connection to other computers.

3.10.1.3
The SIU when resident in a Cabinet Input Assembly controls 24 detector channel inputs (2 channels per slot), 6 detector reset outputs (2 slots per reset line), and 24 detector restart outputs. When resident in an output assembly, it controls up to 14 Model 200 Switch Pack Units (42 outputs). A ground true signal at the DIN 96P Connector Pin C32 shall cause the SIU to operate in the ITS configuration.

3.10.1.4
The SIU requirements match Chapter 9 Section 3 here in called out. Substitute SIU where F I/O and FCU (Field Controller Unit) are called out. The CPU Module references to the 2070 Unit CPU Module.

3.10.2 SIU CONTROLLER UNIT

3.10.2.1
The SIU CONTROLLER UNIT shall include a Microprocessor/Controller Unit; a Loss of Communications Timer, Memory and all required clocking and support circuitry.

3.10.2.2
The LOSS OF COMMUNICATIONS TIMER shall time the period between the last message Response from the SIU to the current ATC/SIU communication on Serial Bus #1. Timer accuracy shall be ± 10 ms. A loss of communications between the ATC/SIU for (2) seconds shall cause a time out. The LOS shall set the E Bit flag and shall blank all field outputs. The timer shall be reset at power up or if time-out has not occurred when the ATC Command communications arrives. At Power Up the SIU shall see the E Flag set indicating loss of Communications until the user program sends the Request Module Status Message to reset the E Bit and reset the Timer. This means that the Response Message says that E is clear (done). The recovery operation is processed by the user software.

The outputs from the Input tracking Functions and Complex Output Functions shall not be allowed to the output connector until the above conditions are met. As long as time out is not timed out, the Status and other messages are allowed to happen. WDT switch and other

output operations are not subject to conditions outlined for Comm loss recovery at Power Up.

3.10.2.3
SIU CONTROLLER UNIT shall be RESET by any of the following:

Reset Push-button Switch
NRESET Signal
Internal +5 VDC out of regulation
SIU Watchdog Circuit

3.10.2.3.1
A Watchdog Circuit shall be provided. The SIU shall power up with the watchdog enabled. Within the first watchdog time period, the watchdog value shall be set to 200 ±100 ms. The watchdog value shall be machine readable and reported in the SIU status byte as an indication that a watchdog has occurred, which will remain until cleared in the Request Module Status command. Failure of the SIU to reset the watchdog timer within 100 ms shall result in hardware reset.

3.10.3 POWER REQUIREMENTS

3.10.3.1
The SIU shall draw no more than 300 ma from the +24 VDC cabinet power supply and shall be insensitive to 700 mV RMS ripple on the incoming +24 VDC line.

3.10.3.2
The SIU shall operate between 18 to 30 VDC. The SIU shall consider 16 VDC or lower for 700 ms. or more as a "Low Power Failure". The SIU shall consider 18VDC or more for 50 ms. as "DC Restored". The SIU shall consider 18 VDC or more by 500 ms as "Return To Normal Operation".

3.10.3.3
At "DC Restored", the SIU loss of communications timer shall indicate loss of communications until the user program sends the Request Module Status message to reset the "E" Bit and a subsequent set output command is processed.

3.10.4 MEMORY - Operational software necessary to meet housekeeping and functional requirements shall be provided resident in socketed firmware or internal Flash memory.

3.10.5 CONTROL SIGNALS
If the NRESET line transitions to logic Low the SIU shall reset its controller unit and communications, blank all outputs and ignore all inputs. If the NRESET line transitions Logic High the SIU shall remain the previous condition until ATC communications are re-established. ATC LINESYNC transitions shall be used as general system timing.

310.6 INTERRUPTS

All interrupts shall be capable of asynchronous operation with respect to all processing and all other interrupts. The SIU includes three interrupt sources as follows:

3.10.6.1

MILLISECOND INTERRUPT - A 1 KHz Time Reference Clock shall be provided to drive a 32-bit Millisecond Counter for "time stamping." Each 1 KHz Clock Interrupt shall increment the Millisecond Counter. The 1KHz Time Reference shall have a frequency accuracy of ±0.01% (±0.1 counts per second). A timestamp rollover flag set by MC rollover shall be cleared only on command.

3.10.6.2

LINESYNC INTERRUPT signal is generated by the controller power supply. LINESYNC Interrupt shall be generated by both the 0-1 and 1-0 transitions of the LINESYNC signal. The LINESYNC interrupt shall monitor the MC interrupt and set the MC error flag if there has not been an interrupt from the 1 KHz source for 0.5 seconds (60 consecutive LINESYNC interrupts). The LINESYNC interrupt shall synchronize the 1 KHz time reference with the 0-1 transition of the LINESYNC signal once a second. A LINESYNC error flag shall be set if the LINESYNC interrupt has not successfully executed for 0.5 seconds or longer (≥500 consecutive millisecond interrupts).

3.10.6.3

The following requirement relates to Unit use in NEMA TS-2 Cabinet only.

LINE FREQUENCY REFFENCE input pin receives a square wave signal from the cabinet power supply for the purposes of synchronizing Unit outputs with the AC line. Line Frequency Reference Interrupt shall be generated by both the 0-1 and 1-0 transitions of the Line Frequency Reference signal. The Line Frequency Reference interrupt shall monitor the MC interrupt and set the MC error flag if there has not been an interrupt from the 1 KHz source for 0.5 seconds (≥60 consecutive Line Frequency Reference interrupts). The Line Frequency Reference interrupt shall synchronize the 1 KHz time reference with the 0-1 transition of the Line Frequency Reference signal once a second. A Line Frequency Reference error flag shall be set if the Line Frequency Reference interrupt has not successfully executed for 0.5 seconds or longer (≥500 consecutive millisecond interrupts). The electrical characteristics of the Line Frequency input are as follows:

3.10.6. 3.1

A voltage between 0 and 8 volts shall be considered the LOW state, and shall occur when the AC line is in the positive half cycle. A voltage between 16 and 26 volts shall be considered the HIGH state, and shall occur when the AC line is in the negative half-cycle.

3.10.6.3.2

The Line Frequency Reference input shall exhibit a nominal impedance of 10 K ± 10% to the +24 VDC input and shall not have more than 1000 picofarads of load capacitance. The rise and fall time of the signal connected to this input shall not exceed 50 microseconds.

3.10.6.3.3
The SIU Enable input is used by the SIU to determine the AC timing source. If the SIU Enable input is grounded, LINESYNC is used as the interrupt source. If the SIU Enable input is pulled up, Line Frequency Reference is used as the interrupt source.

3.10.6.3.4
Note: This Line Frequency Referrals a requirement of NEMA Cabinet only.

3.10.7 TRANSITION BUFFERS
See 9.3.7 Specification "BUFFERS"

3.10.8.1
COMMUNICATION PROCESSING - The task shall be to process the command messages received from the CPU Module, prepare, and start response transmission. The response message transmission shall begin within 4 ms of the receipt of the received message. The SIU shall complete the execution of each command within 70 ms of the end of each response message transmission.

3.10.9 INPUT PROCESSING - This task shall process the raw input data scanned in by the 1 ms interrupt routine, perform all filtering, and maintain the transition queue entries.

3.10.10 INPUTS AND OUTPUTS- The SIU has 4 Optically Coupled Inputs, 54 Parallel Input/Outputs and 4 Serial Ports.

3.10.10.1 OPTICALLY-COUPLED INPUTS
The OPTO-COMMON Input is the common reference pin for the four RAW OPTO-INPUTS. The RAW OPTO-INPUTS are intended to provide optical isolation for pedestrian detection, internal cabinet functions, Remote Interconnect or other auxiliary inputs. The Raw Opto Inputs are intended to connect through external 27K ohm, 1-Watt resistors for 120 VAC operations, and are intended for direct connection to 12 VAC for Pedestrian Detector applications. These inputs may also be used for low-true DC applications when the Opto Common pin is connected to +24 VDC.

3.10.10.1.1
The Raw Opto Inputs shall provide electrical isolation of 10 megohms minimum resistance and 1000 VAC RMS minimum breakdown to all connector pins except the Opto Common pin, at a maximum breakdown leakage current of 1 mA RMS. These inputs shall exhibit nominal impedance to the Opto Common pin of 5000 ohms, +10% to the Opto Common input.

3.10.10.1.2
The Raw Opto Inputs shall not recognize 3 volts RMS (AC sinusoid or DC) or less relative to the Opto Common input. The Raw Opto Inputs shall recognize 8 volts RMS (AC sinusoid or DC) or more relative to the Opto Common input. Any steady state voltage applied between an Opto Input and the Opto Common shall not exceed 35 VAC RMS. Raw Opto Inputs shall not be acknowledged when active for 25 ms or less, and shall be acknowledged when active for 50 mS or more. The Opto Inputs shall conform to transient

immunity specifications of paragraph 1.8.4.4. The first Input and first Output Assembly assignments are dedicated as follows:

PIN	1st INPUT ASSEMBLY	1ST OUTPUT ASSEMBLY
Raw Opto Input 1	Manual Flash Enable	Door Ajar
Raw Opto Input 2	Manual Enable	Monitor Interlock
Raw Opto Input 3	Interval Advance	(not assigned)
Raw Opto Input 4	(reserved for Stop Time)	
Raw Opto Input Gnd		

3.10.10.2 PARALLEL INPUTS AND OUTPUTS - SIU shall control 54 input/output lines using ground-true logic.

3.10.10.2.1 INPUT SECTION - Each input shall be read logic "1" when the input voltage at its field connector input is less than 8 VDC, and shall be read logic "0" when the input voltage exceeds 16 VDC. Each input shall have an internal pull-up to +24 VDC of 11K ohms maximum, and shall not deliver greater than 10 mA to a short circuit to ground.

3.10.10.2.2 OUTPUT SECTION - Each output written as a logic "1" shall have a voltage at its field connector output of less than 4.0 VDC. Each output written as logic "0" shall provide an open circuit (1 megohm or more) at its field connector output. Each output shall consist of an open-collector capable of driving 40 VDC minimum and sinking 100 mA minimum. Each output circuit shall be capable of switching from logic "1" to logic "0" within 100 μs when connected to a load of 100 K-Ohms minimum. Each output circuit shall be protected from transients of 10 ±2 μs duration, ±300 VDC from a 1 K-Ohm source, with a maximum rate of 1 pulse per second. Each output shall latch the data written and remain stable until either new data is written or the active-low reset signal. Upon an active-low reset signal, each output shall latch a logic "0" and retain that state until a new writing. The state of all output circuits at the time of Power Up or in Power Down state shall be open. It shall be possible to simultaneously assert all outputs within 100 μs of each other. An output circuit state not changed during a new writing shall not glitch when other output circuits are updated.

3.10.10.3 INPUT/OUTPUT FUNCTIONS - See Specification 9.3.8

3.10.11 SERIAL PORTS

The SIU shall have a minimum of four serial ports, identified as SIU Ports 1-4. Serial Ports 1 and 3 are connected to the SIU microprocessor/controller unit, while Serial Ports 2 and 4 provide a buffered communications path from the ATC to the detectors, and are not connected to the microprocessor/controller unit. Communications circuitry shall be capable of 614.4 Kbps of reliable data pass through.

3.10.11.1 SIU PORT 1 OPERATION

Port 1 shall interface the SIU to Serial Bus 1 of the ITS cabinet Modular Bus Assemblies. All communications circuitry and protocol shall match Serial Bus 1 requirements. The SIU shall function as the "LOCAL" command node for this network responding with appropriate action. See ATC specification sections 2 & 3, CPU Field I/O, for protocol and

requirements. The SP5 SDLC frame address assignments (Command/Responses) are as follows:

Address		A7	A6	A5	A4	A3	A2	A1	A0
1	14-pack in position 1	0	0	0	0	0	0	0	1
2	14-pack in position 3	0	0	0	0	0	0	1	0
3	Reserved	0	0	0	0	0	0	1	1
4	6-pack in position 4	0	0	0	0	0	1	0	0
5	6-pack in position 1	0	0	0	0	0	1	0	1
6	6-pack in position 2	0	0	0	0	0	1	1	0
7	6-pack in position 3	0	0	0	0	0	1	1	1
8	Reserved	0	0	0	0	1	0	0	0
9	Input #1	0	0	0	0	1	0	0	1
10	Input #2	0	0	0	0	1	0	1	0
11	Input #3	0	0	0	0	1	0	1	1
12	Input #4	0	0	0	0	1	1	0	0
13	Input #5	0	0	0	0	1	1	0	1
14	Reserved	0	0	0	0	1	1	1	0
15	CMU	0	0	0	0	1	1	1	1
16	Reserved	0	0	0	1	0	0	0	0
17	Reserved	0	0	0	1	0	0	0	1
18	Reserved	0	0	0	1	0	0	1	0
19	CPU	0	0	0	1	0	0	1	1
20	FIO 2A or 8	0	0	0	1	0	1	0	0
21	To 126 & 128-255 Reserved								
127	Broadcast All	0	1	1	1	1	1	1	1

Note 1: A0 to A3 are Input to SIU with DC ground as common.
Note 2: 0= open or ground false. 1= closed or ground true (shunted)

3.10.11.2 SIU PORT 2 OPERATION

SIU Port 2 shall interface to Serial Bus 2 of the ITS cabinet Modular Bus Assemblies providing a communications path to the ATC for block data retrieval. No connection exists between SIU Port 1 and SIU Port 2. Similarly, no connection exists between SIU Port 2 and the microprocessor/controller unit. All data transfers between SIU Ports 1 and 2 shall be accomplished by the ATC. Data sent back shall include monitor diagnostic status and communication status; input diagnostics status (detector sensor or isolator); and processed

channel inputs data such as rate counts, occupancies, average speeds, speed classification and incident/presence.

Synchronous Operation

If the ATC is communicating via Logical Port SP3S, SIU Port 2 shall communicate in SDLC format and protocol, and the hardware requirements shall match Serial Bus 2 (synchronous TX/RX using TX Clock from the ATC CPU for common clocking).

Asynchronous Operation

If the ATC is communicating via Logical Port SP3, SIU Port 2 shall communicate in an asynchronous START BIT / STOP BIT format and protocol.

3.10.11.3 SIU PORT 3 OPERATION

The SIU Port 3 shall be provided for communication an IBM PC via a front panel DB-9 connector and EIA-232 logic. Its purpose is to upload diagnostic information, and to download the SIU program. The SIU Port 3 protocol shall be defined by the vendor, and operate with vendor-supplied software running on an IBM PC under Windows 98 or Windows NT. The pin assignments of SIU Port 3 shall match that of ATC C60.

3.10.11.4 SIU PORT 4 OPERATION

SIU Port 4 consists of Detector Rack signal INBUS TxD, INBUS RxD, INBUS TxC, and INBUS RxC, and shall conform to the electrical standards of EIA-485, single-ended. In this scheme, the RxD- and RxC- inputs of the EIA-485 receivers are connected to 2.5 volts, while the TxD- and TxC- outputs of the EIA-485 drivers are not used. SIU Port 4 receivers shall withstand ± 25 volts, suitable for reception of EIA-232 bipolar signals. All four INBUS signals shall be terminated at each receiver with impedance of 6800 ± 5 % ohms, connected from signal to +5V Ground on the SIU. The detector vendor shall define the SIU Port 4 protocol. The SIU provides one inversion to insure a controller MARK equates to a detector MARK. The SIU shall provide an LED indicator for TxD and RxD, such that is illuminated during a MARK (START Bit, for example) and extinguished during a SPAC (STOP Bit, for example). SIU Port 4 provides buffering to SIU Port 2, allowing the ATC to communicate directly to the detectors, as follows:

3.10.11.5 SYNCHRONOUS OPERATION

If the ATC is communicating to detectors via Logical Port SP3S, the SIU Port 4 buffers convert SIU Port 2 TxD+ and TxD- to EIA-485 which is then transmitted to the detectors via INBUS TxD. Likewise, the SIU Port 4 buffers convert SIU Port 2 TxC+ and TxC- to EIA-485 and which is then transmitted to the detectors via INBUS TxC. If the ATC is communicating to detectors via Logical Port SP3S, the SIU Port 4 buffers convert INBUS RxD from EIA-485, which is then transmitted to the ATC via SIU Port 2 RxD+ and RxD-. Likewise, the SIU Port 4 buffers convert INBUS RxC from EIA-485, which is then transmitted to the ATC via SIU Port 2 RxC+ and RxC-.

3.10.11.6 ASYNCHRONOUS OPERATION

If the ATC is communicating to detectors via Logical Port SP3, the SIU Port 4 buffers convert SIU Port 2 TxD+ and TxD- to EIA-485 which is transmitted to the detectors via INBUS TxD. If the ATC is communicating to detectors via Logical Port SP3, the SIU Port 4 buffers convert INBUS RxD is from EIA-485, which is transmitted to the ATC via SIU Port 2 RxD+ and RxD- Asynchronous operation does not use Port 2 TxC+, TxC-, RxC+, RxC-, nor Port 4 INBUS TxC, or INBUS RxC.

3.10.11.7 INPUT ASSEMBLY ADDRESS

The SIU senses the address and generates a square wave on the ASSEMBLY ADDRESS signal as follows:

Assembly Address	Assembly Address Frequency (Hz) +/- 5%
9	60
10	30
11	15
12	7.5
13	3.75

3.10.11.8 INBUS RTS INPUT

The INBUS RTS line is pulled to +24V via a 10 K ohm resistor on the SIU. In systems using legacy detectors that do not use INBUS RTS, this line is not used (no connection). Detectors equipped with INBUS RTS shall drive this line low when transmitting data from that detector to the SIU via INBUS. When not transmitting data, this line is not driven low and is pulled to +24V via the 10K ohm resistor.

3.10.11.8.1 SERIAL BUS 2 CONTROL

The controller transmits a message on Serial Bus 2 that is received by each detector via the SIU INBUS TxD and INBUS TxC. If the detector is asynchronous, INBUS TxC is ignored. Each detector compares the address field of the message with its own slot address and assembly address. If the address matches, that detector responds with data on INBUS RxD and INBUS RxC. If the detector is asynchronous, INBUS RxC is not used. The SIU of the responding detector enables its EIA-485 line drivers to transmit the response from INBUS to SB2. This driver is enabled by any of the three following conditions:

1. **Activity on INBUS RxD**
2. **Activity on INBUS RxC**
3. **INBUS RTS at 0 volts**

This driver is disabled by either of the following two conditions:

1. **Lack of activity on both INBUS RxD and RxC for 1.5 mS**
2. **Inbus RTS transitions from 0 to +24 V.**

3.10.12 COMMUNICATION PROTOCOL

See Specification 9.3.9 except for the following:

9.3.9.1	**Protocols**	**Add Message Frames 65 /193 for Cabinet Monitor Unit. Remove from Reserved.**
9.3.9.2	**Request Module Status**	**Watchdog Status "W" not required.**
9.3.9.4 & 9.3.9.7		**Input Number 0 to 53**
9.3.9.5		**Includes 4 Opto Inputs**
9.3.9.6		**SIU always includes 8 Bytes of Data**
9.3.9.8		**8 Bytes of Data and 8 Bytes of Control**
9.3.9.11 & .12		**Not required**
9.3.9.13		**Use SIU PORT 1 Operation Addressing for Identification**

3.10.13 ADDRESS SELECT INPUTS

Address Select Inputs - The Address Select input bits define the logical position of each SIU. No connection is logical False, while a connection to Logic Ground is a logical True. There shall be 16 unique address positions selected with a binary code, using bit 0 as least significant and bit 3 as most significant.

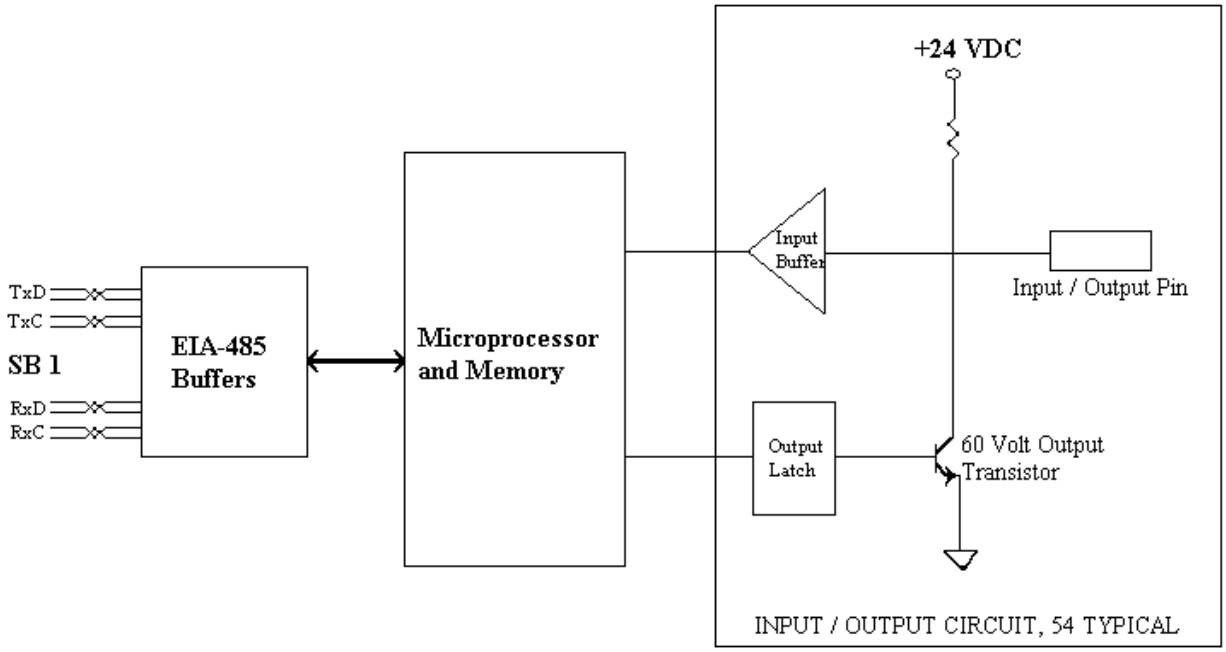
3.10.14 SIU INPUT and OUTPUT ASSIGNMENTS

SIU	Set Output Command 55		Raw Data Input Response 180		SIU	Set Output Command 55		Raw Data Input Response 180	
I/O 0	Byte 2	Bit 0	Byte 2	Bit 0	I/O 32	Byte 6	Bit 0	Byte 6	Bit 0
I/O 1		Bit 1		Bit 1	I/O 33		Bit 1		Bit 1
I/O 2		Bit 2		Bit 2	I/O 34		Bit 2		Bit 2
I/O 3		Bit 3		Bit 3	I/O 35		Bit 3		Bit 3
I/O 4		Bit 4		Bit 4	I/O 36		Bit 4		Bit 4
I/O 5		Bit 5		Bit 5	I/O 37		Bit 5		Bit 5
I/O 6		Bit 6		Bit 6	I/O 38		Bit 6		Bit 6
I/O 7		Bit 7		Bit 7	I/O 39		Bit 7		Bit 7
I/O 8	Byte 3	Bit 0	Byte 3	Bit 0	I/O 40	Byte 7	Bit 0	Byte 7	Bit 0
I/O 9		Bit 1		Bit 1	I/O 41		Bit 1		Bit 1
I/O 10		Bit 2		Bit 2	I/O 42		Bit 2		Bit 2
I/O 11		Bit 3		Bit 3	I/O 43		Bit 3		Bit 3
I/O 12		Bit 4		Bit 4	I/O 44		Bit 4		Bit 4
I/O 13		Bit 5		Bit 5	I/O 45		Bit 5		Bit 5
I/O 14		Bit 6		Bit 6	I/O 46		Bit 6		Bit 6
I/O 15		Bit 7		Bit 7	I/O 47		Bit 7		Bit 7
I/O 16	Byte 4	Bit 0	Byte 4	Bit 0	I/O 48	Byte 8	Bit 0	Byte 8	Bit 0
I/O 17		Bit 1		Bit 1	I/O 49		Bit 1		Bit 1
I/O 18		Bit 2		Bit 2	I/O 50		Bit 2		Bit 2
I/O 19		Bit 3		Bit 3	I/O 51		Bit 3		Bit 3
I/O 20		Bit 4		Bit 4	I/O 52		Bit 4		Bit 4
I/O 21		Bit 5		Bit 5	I/O 53		Bit 5		Bit 5
I/O 22		Bit 6		Bit 6	Active LED		Bit 6		Bit 6
I/O 23		Bit 7		Bit 7	Opto In 1	56			Bit 7
I/O 24	Byte 5	Bit 0	Byte 5	Bit 0	Opto In 2	57		Byte 9	Bit 0
I/O 25		Bit 1		Bit 1	Opto In 3	58			Bit 1
I/O 26		Bit 2		Bit 2	Opto In 4	59			Bit 2
I/O 27		Bit 3		Bit 3	A000				Bit 3
I/O 28		Bit 4		Bit 4	A001				Bit 4
I/O 29		Bit 5		Bit 5	A002				Bit 5
I/O 30		Bit 6		Bit 6	A003				Bit 6
I/O 31		Bit 7		Bit 7					Bit 7

NOTE:
A000 to A003 is the address of the SIU, useful when saving the response for later identification.

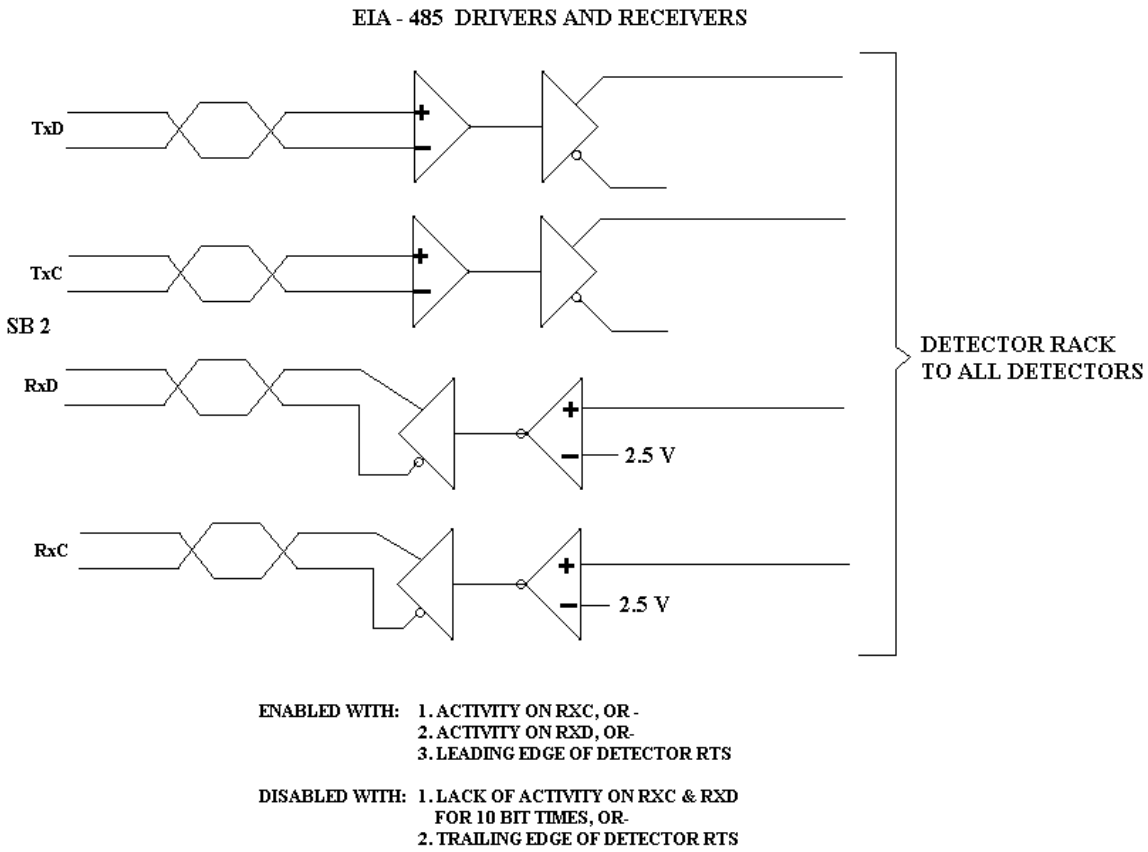
3.10.15 SIU STRUCTURE

Each SIU contains 54 Input/Outputs, each connected as follows:



When the SIU is powered, all outputs are initialized OFF and 54 inputs are available. Without jumpers or firmware changes, the Controller software can simply turn on any of the 54 outputs. Each output can be read back as an input to check integrity.

3.10.16 SIU / SERIAL BUS 2 AND DETECTORS



This circuitry is included in each SIU, providing a direct serial connection from the controller to each individual serial detector. This serial connection is in addition to all of the NEMA CALL and STATUS lines shown in Case 2.

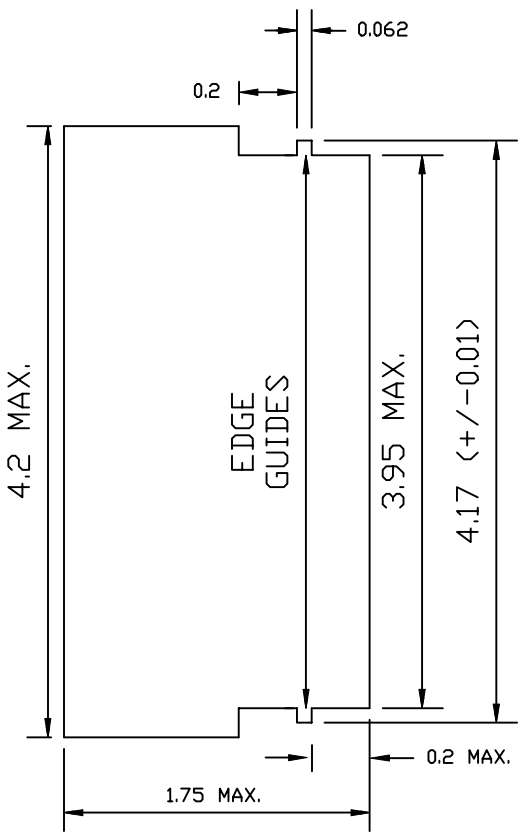
CHAPTER 3 SECTION 11
CHAPTER DETAILS

TABLE OF CONTENTS

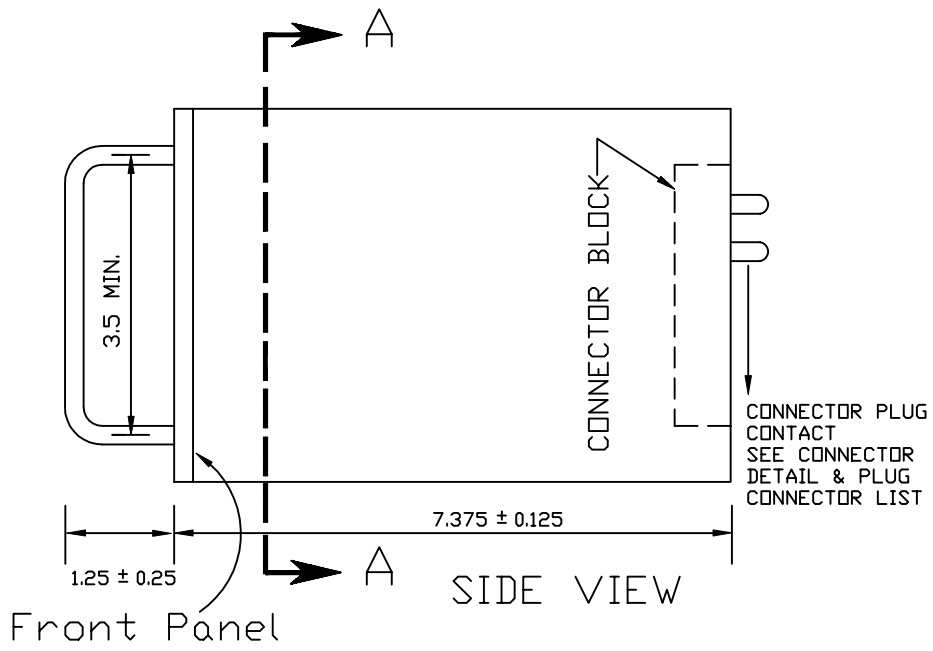
Section Notes:

All measurements shall be in inches.

MODEL 200 SWITCH PACK & 204 FLASHER UNITS



CROSS SECTION A-A



MODEL PLUG CONNECTORS LIST
(OR EQUAL)

MODEL 200 - BEAU P-5412-LAB
MODEL 204 - BEAU P-5406-LAB
MODEL 205 - BEAU P-5408-LAB
MODEL 206 - BEAU P-5406-LAB

MODEL 200, 204, 205, 206 CONNECTOR DETAIL

PIN	FUNCTION
1	AC+
2	Equip. Ground
3	Red Output
4	Not Assigned
5	Yellow Output
6	Red Input
7	Green Output
8	Yellow Input
9	+24 VDC
10	Green Input
11	Not Assigned
12	Not Assigned

PIN	FUNCTION
7	Load Circuit #1
8	Load Circuit #2
9	Equip. Ground
10	AC-
11	AC+
12	Not Assigned

PIN	Function
1	Coil
2	Coil
3	NC CKT1
4	NC CKT2
5	Common CKT1
6	Common CKT2
7	NO CKT1
8	NO CKT2

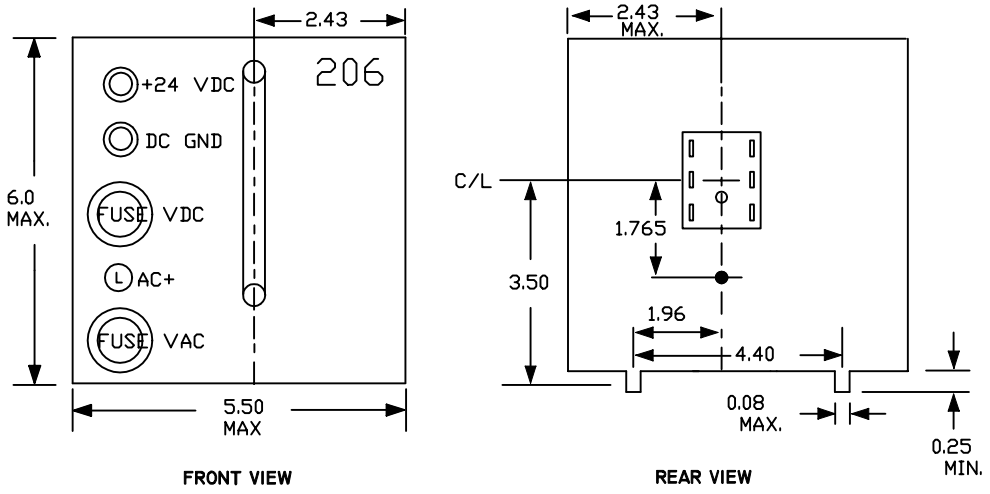
TITLE:
MODEL 200 SWITCH PACK
& 204 FLASHER UNITS

NO SCALE

MARCH 29, 2002

3-11-1

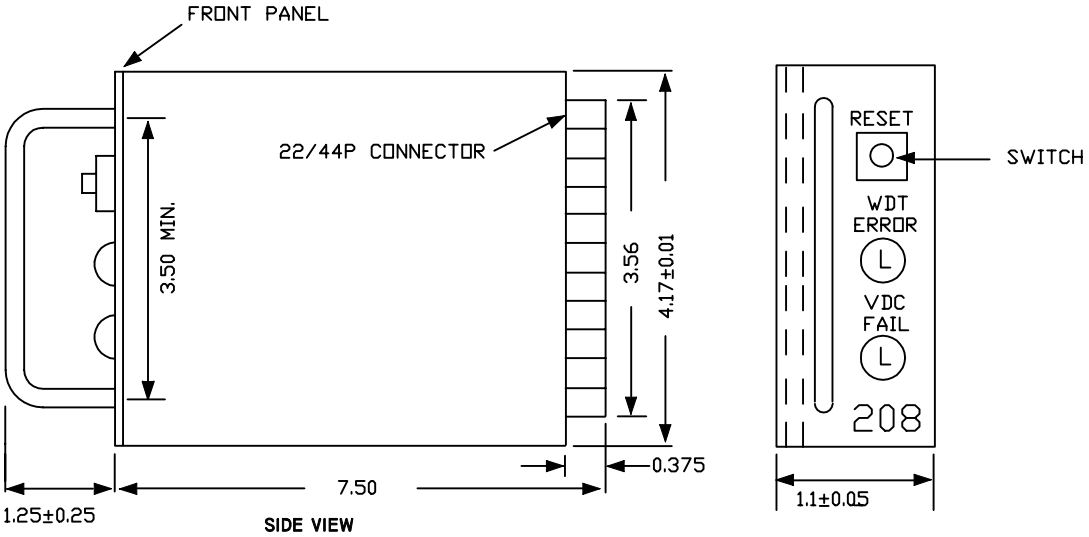
MODEL 206 TI70 CABINET POWER SUPPLY UNIT



MODEL PLUG CONNECTORS LIST (OR EQUAL)

MODEL 200 - BEAU P-5412-LAB
MODEL 204 - BEAU P-5406-LAB
MODEL 205 - BEAU P-5408-LAB
MODEL 206 - BEAU P-5406-LAB

MODEL 208 TI70 TMU MONITOR UNIT



MODEL 208 MONITOR UNIT PIN ASSIGNMENT

PIN	FUNCTION
1/A	WDT Lamp (External)
2/B	Circ. Common # 1 & # 2
3/C	Normally Closed, Circ. # 1
4/D	AC+
6/F	Normally open, Circ. # 2

PIN	FUNCTION
8/J	AC-
13/P	+24 VDC
18/V	WDT IN
21/Y	WDT Ext. Reset
22/Z	DC Ground

"U" SHAPED ROD HANDLE FABRICATED OF 0.25 +/- 0.05 DIAMETER, ALUMINUM STOCK, WITH 4.0 +/- 0.125 LENGTH, & ROD CENTER TO CENTER, SHALL BE PROVIDED. THE HANDLE SHALL BE VERTICALLY CENTERED. THE DEPTH FROM THER VERTICAL CENTERLINE OF THE HANDLE ROD TO THE MODULE FRONT PANEL SHALL BE 1.25 +/- 0.125

THE POWER SUPPLY UNIT DIMENSION, FROM FRONT PANEL TO CONNECTOR PLUG, SHALL BE 7.375 + 0.000, -0.125

A STANDARD 8-32 METAL STUD RETAINING SCREW SHALL PROVIDE PROPER SECURING OF THE POWER SUPLY WHEN INSTALLED IN THE PDA USING WASHERS AND A WINGNUT. WHEN TORQUED IN THE LOCKING POSITION NO STRESS SHALL BE APPLIED ON THE MATING SOCKET/PLUG CONNECTOR SURFACE. NO MOUNTING OF CHASSIS SUPPORT SCREWS SHALL PROTRUDE BEYOUND THE MATING SURFACE OF THE POWER SUPPLY CONNECTORS.

TITLE:

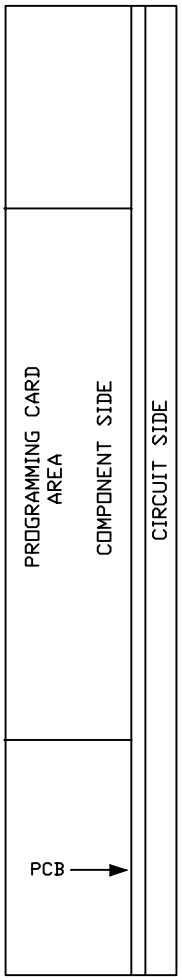
MODEL 206 CABINET POWER SUPPLY & 208 TMU MONITOR UNITS

NO SCALE

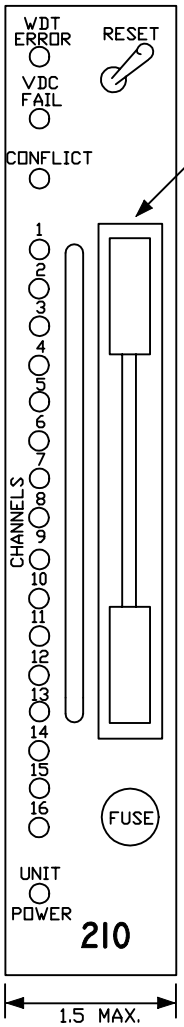
MARCH 29, 2002

3-11-2

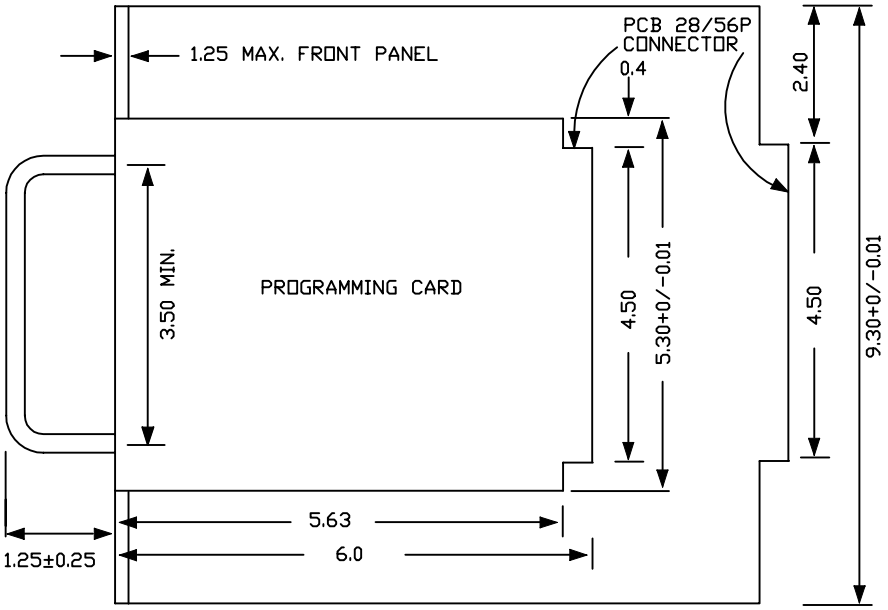
MODEL 210 MONITOR UNIT



REAR VIEW



FRONT VIEW



SIDE VIEW

TITLE: MODEL 210 T170 MONITOR UNIT	
NO SCALE	3-11-3
MARCH 29, 2002	

MODEL 210 MONITOR UNIT CONNECTOR WIRING ASSIGNMENTS

Pin	FUNCTION	Pin	FUNCTION
1	Channel #2 Green	A	Channel #2 Yellow
2	Channel #13 Green	B	Channel #6 Green
3	Channel #6 Yellow	C	Channel #15 Green
4	Channel #4 Green	D	Channel #4 Yellow
5	Channel #14 Green	E	Channel #8 Green
6	Channel #8 Yellow	F	Channel #16 Green
7	Channel #5 Green	H	Channel #5 Green
8	Channel #13 Yellow	J	Channel #1 Green
9	Channel #1 Yellow	K	Channel #15 Yellow
10	Channel #7 Green	L	Channel #7 Yellow
11	Channel #14 Yellow	M	Channel #3 Green
12	Channel #3 Yellow	N	Channel #16 Yellow
13	Channel #9 Green	P	NA
14	NA	R	Channel #10 Green
15	Channel #11 Yellow	S	Channel #11 Green
16	Channel #9 Yellow	T	NA
17	NA	U	Channel #10 Yellow
18	Channel #12 Yellow	V	Channel #12 Green
19	NA	W	NA
20	Equipment Ground	X	NA
21	AC– *	Y	DC Ground
22	Watchdog Timer	Z	External Reset
23	+24 VDC	AA	+24 VDC
24	(Pins 24 & 25	BB	Stop Time
25	Tied Together)	CC	NA
26	NA	DD	NA
27	NA	EE	Output SW, Side #2
28	Output SW, Side #1	FF	AC+

MODEL 210 PROGRAMMING CARD CONNECTOR WIRING ASSIGNMENTS

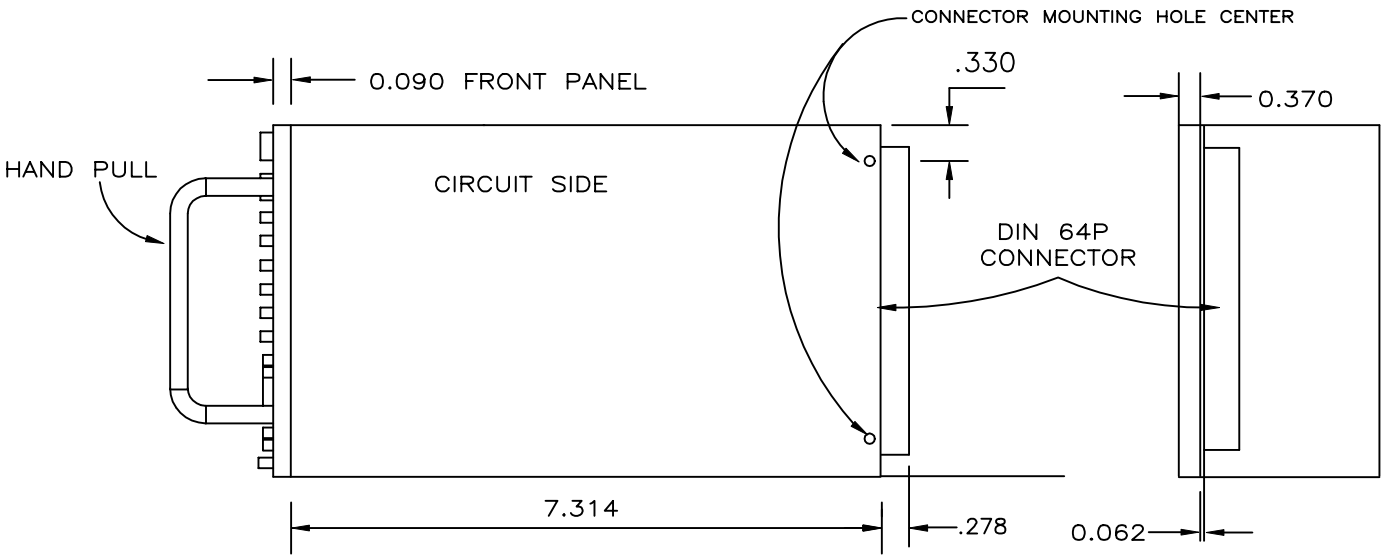
Pin	FUNCTION (Circuit Side)	Pin	FUNCTION (Component Side)
1	Channel #2 Green	A	Channel #1 Green
2	Channel #3 Green	B	Channel #2 Green
3	Channel #4 Green	C	Channel #3 Green
4	Channel #5 Green	D	Channel #4 Green
5	Channel #6 Green	E	Channel #5 Green
6	Channel #7 Green	F	Channel #6 Green
7	Channel #8 Green	H	Channel #7 Green
8	Channel #9 Green	J	Channel #8 Green
9	Channel #10 Green	K	Channel #9 Green
10	Channel #11 Green	L	Channel #10 Green
11	Channel #12 Green	M	Channel #11 Green
12	Channel #13 Green	N	Channel #12 Green
13	Channel #14 Green	P	Channel #13 Green
14	Channel #15 Green	R	Channel #14 Green
15	Channel #15 Green	S	Channel #15 Green
16	DC Ground	T	CONFLICT
17	Channel #1 Yellow	U	Channel #9 Yellow
18	Channel #2 Yellow	V	Channel #10 Yellow
19	Channel #3 Yellow	W	Channel #11 Yellow
20	Channel #4 Yellow	X	Channel #12 Yellow
21	Channel #5 Yellow	Y	Channel #13 Yellow
22	Channel #6 Yellow	Z	Channel #14 Yellow
23	Channel #7 Yellow	AA	Channel #15 Yellow
24	Channel #8 Yellow	BB	Channel #16 Yellow
25	NA	CC	NA
26	NA	DD	NA
27	NA	EE	Output SW, Side #2
28	Output SW, Side #1	FF	AC+

TITLE: MODEL 210 MONITOR UNIT & PROGRAMMING CARD CONNECTOR WIRING ASSIGNMENTS

NO SCALE

MARCH 29, 2002

3–11–4

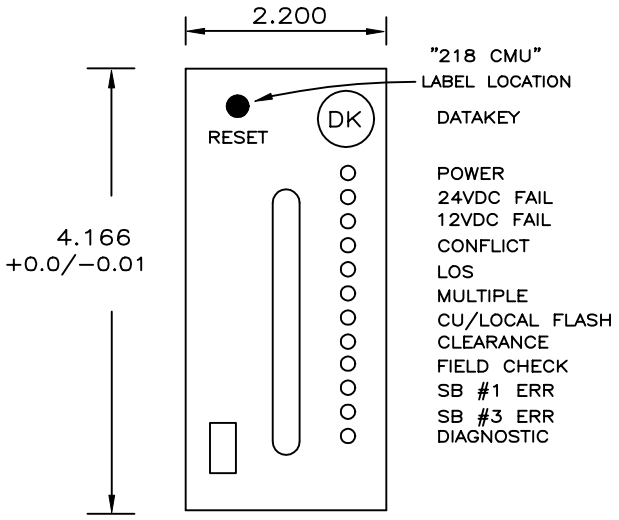


SIDE VIEW

END VIEW

DIN 64P PIN ASSIGNMENTS

Pin #	FUNCTION	Pin #	FUNCTION
A1	+24 VDC in	B1	NA
A2	+12 VDC in	B2	External Reset
A3	VDC Ground	B3	RESERVED (Test)
A4	Monitor Interlock	B4	NA
A5	NA	B5	NA
A6	NA	B6	NA
A7	SB1 TxD+	B7	SB1 TxD−
A8	SB1 RxD+	B8	SB1 RxD−
A9	SB1 TxC+	B9	SB1 TxC−
A10	SB1 RxC+	B10	SB1 RxC−
A11	NA	B11	NA
A12	NA	B12	NA
A13	NA	B13	NA
A14	NA	B14	NA
A15	LINESYNC.+	B15	LINESYNC.−
A16	NRESET+	B16	NRESET−
A17	PWRDOWN+	B17	PWRDOWN−
A18	SB3 TxD+	B18	SB3 TxD−
A19	SB3 RxD+	B19	SB3 RxD−
A20	SB3 TxC+	B20	SB3 TxC−
A21	LFSA IN	B21	LFSA IN
A22	LFSA OUT	B22	LFSA OUT
A23	CB Trip Status	B23	NA
A24	MC Coil	B24	NA
A25	MC Secondary	B25	NA
A26	FTR Coil	B26	NA
A27	Door Switch Front	B27	NA
A28	Door Switch Rear	B28	NA
A29	NA	B29	NA
A30	NA	B30	AC+ RAW
A31	EQ Ground	B31	NA
A32	NA	B32	AC− RAW



FRONT VIEW

NOTES:

- ○ −LED INDICATOR
- ● −MOMENTARY PUSH BUTTON SWITCH
- ▭ −DB9S CONNECTOR
- SB −SERIAL BUS

MC −MAIN CONTACTOR
FTR −FLASH TRANSFER RELAY
NA −NOT APLICABLE
LFSA −LATCHED FAIL STATE ACTION

PORT 4 PIN ASSIGNMENT (DB9S)

1 NA	6 NA
2 RxD	7 NA
3 TxD	8 NA
4 NA	9 NA
5 DC GND	

TITLE:

MODEL 212 CABINET MONITOR UNIT (CMU) DETAILS

NO SCALE

MARCH 29, 2002

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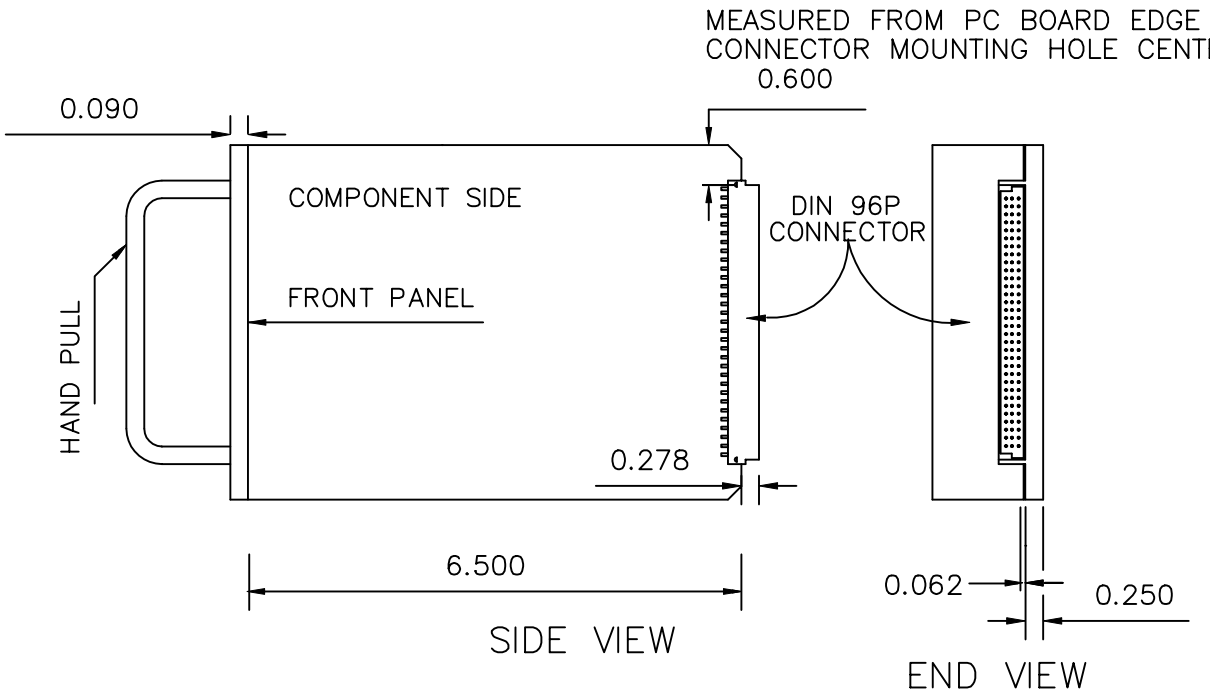
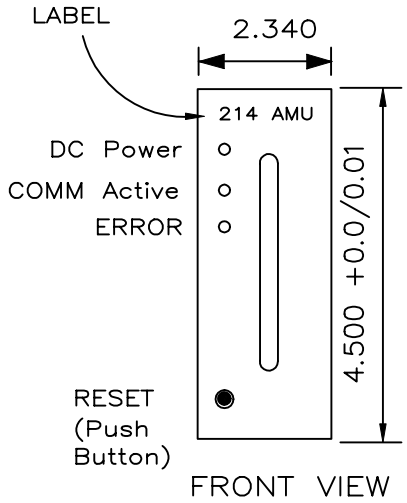


DIN 96P PIN ASSIGNMENTS

Pin #	FUNCTION	Pin #	FUNCTION	Pin #	FUNCTION
A1	VDC Ground	B1	+24 VDC in	C1	Address Common
A2	SB3 RxC+	B2	SB3 TxD−	C2	SB3 TxD+
A3	SB3 RxC−	B3	SB3 RxD−	C3	SB3 RxD+
A4	ADDR 0	B4	ADDR 1	C4	ADDR 2
A5	I Coil 3+	B5	I Coil 2+	C5	I Coil 1+
A6	I Coil 3−	B6	I Coil 2−	C6	I Coil 1−
A7	I Coil 6+	B7	I Coil 5+	C7	I Coil 4+
A8	I Coil 6−	B8	I Coil 5−	C8	I Coil 4−
A9	I Coil 9+	B9	I Coil 8+	C9	I Coil 7+
A10	I Coil 9−	B10	I Coil 8−	C10	I Coil 7−
A11	I Coil 12+	B11	I Coil 11+	C11	I Coil 10+
A12	I Coil 12−	B12	I Coil 11−	C12	I Coil 10−
A13	I Coil 14+	B13	I Coil 13−	C13	I Coil 13+
A14	I Coil 14−	B14	FU2−1	C14	FU1−1
A15	NA	B15	FU2−2	C15	FU1−2
A16	Switchpack 1 Green	B16	Switchpack 1 Yellow	C16	Switchpack 1 Red
A17	Switchpack 2 Green	B17	Switchpack 2 Yellow	C17	Switchpack 2 Red
A18	Switchpack 3 Green	B18	Switchpack 3 Yellow	C18	Switchpack 3 Red
A19	Switchpack 4 Green	B19	Switchpack 4 Yellow	C19	Switchpack 4 Red
A20	Switchpack 5 Green	B20	Switchpack 5 Yellow	C20	Switchpack 5 Red
A21	Switchpack 6 Green	B21	Switchpack 6 Yellow	C21	Switchpack 6 Red
A22	Switchpack 7 Green	B22	Switchpack 7 Yellow	C22	Switchpack 7 Red
A23	Switchpack 8 Green	B23	Switchpack 8 Yellow	C23	Switchpack 8 Red
A24	Switchpack 9 Green	B24	Switchpack 9 Yellow	C24	Switchpack 9 Red
A25	Switchpack 10 Green	B25	Switchpack 10 Yellow	C25	Switchpack 10 Red
A26	Switchpack 11Green	B26	Switchpack 11 Yellow	C26	Switchpack 11 Red
A27	Switchpack 12 Green	B27	Switchpack 12 Yellow	C27	Switchpack 12 Red
A28	Switchpack 13 Green	B28	Switchpack 13 Yellow	C28	Switchpack 13 Red
A29	Switchpack 14 Green	B29	Switchpack 14 Yellow	C29	Switchpack 14 Red
A30	NA	B30	AC+ RAW	C30	AC+ RAW
A31	EQ Ground	B31	NA	C31	NA
A32	NA	B32	AC− RAW	C32	AC− RAW



Notes:

○ − LED indicator

◉ − Recessed Momentary Push Button Switch

I−Coil−Current Sense Coil
SB −Serial Bus Coil
NA −Not Applicable

TITLE:

MODEL 214 AUXILLARY MONITOR UNIT (AMU) DETAILS

NO SCALE

MARCH 29, 2002

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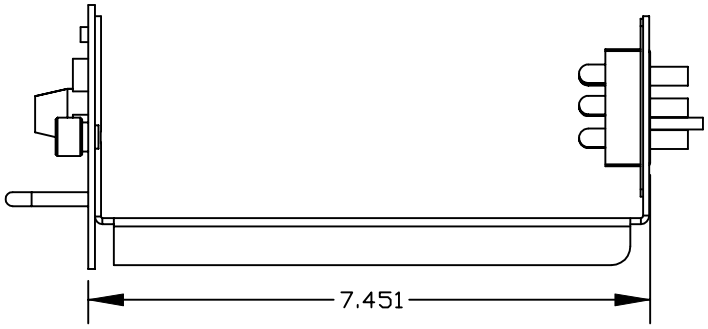
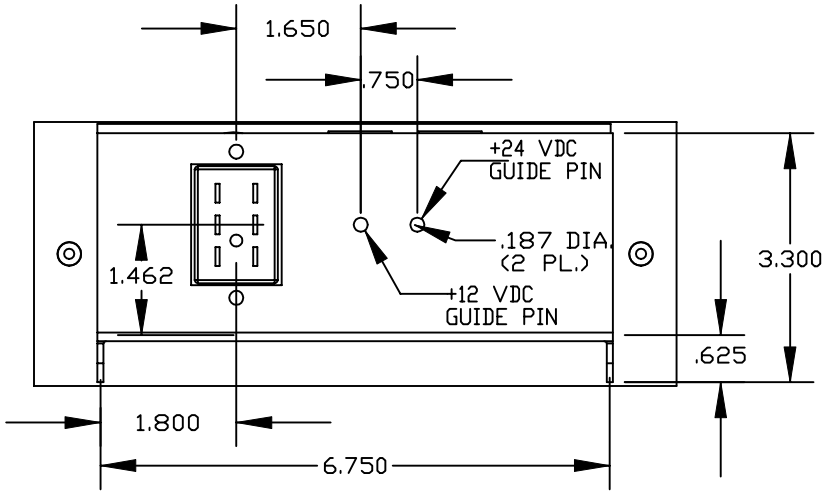


SIDE VIEW



REAR VIEW

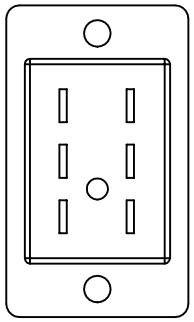
TITLE:

MODEL 216 ITS CABINET POWER SUPPLY UNIT

NO SCALE

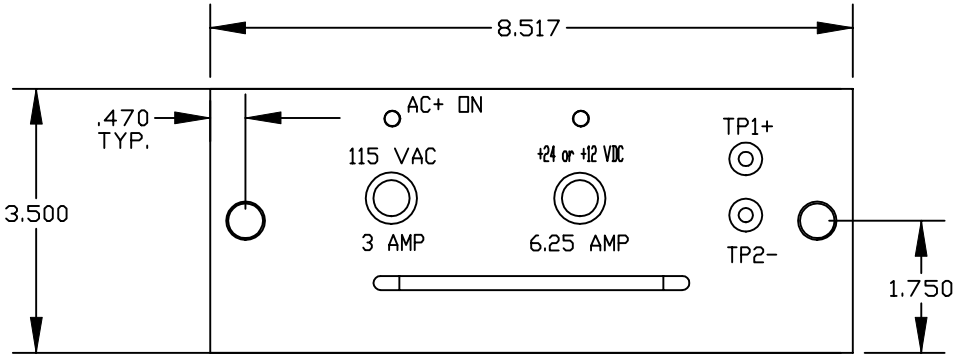
MARCH 29, 2002

3-11-7



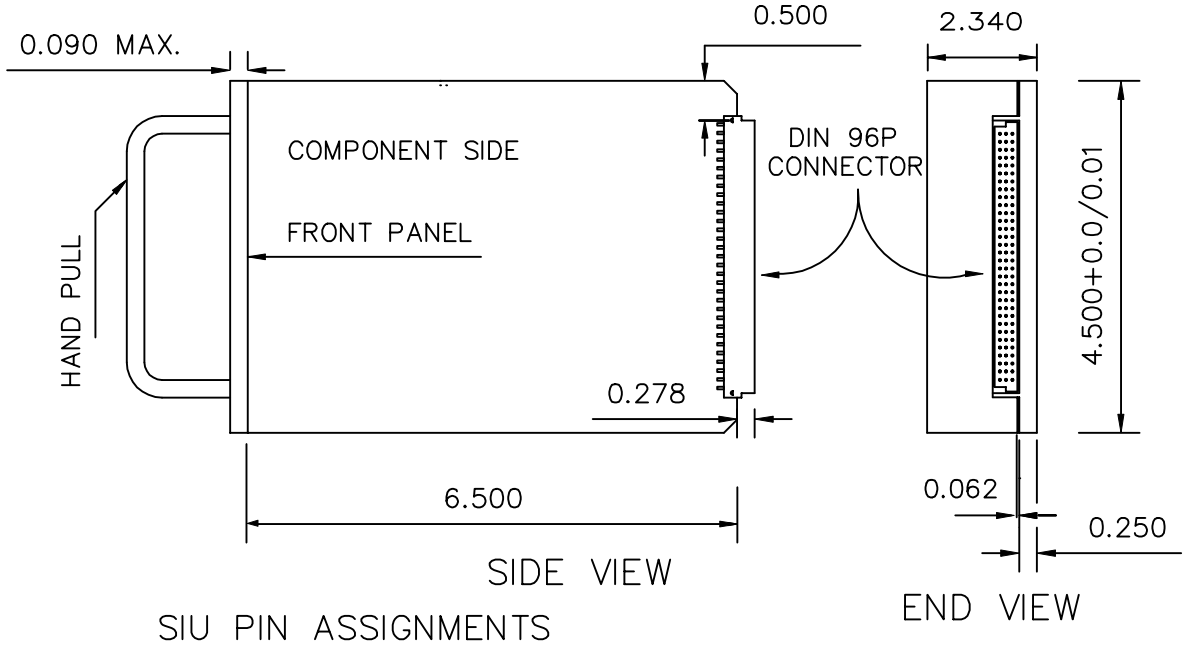
SOCKET FRONT VIEW

7	+24 VDC	8	+12 VDC
9	DC GROUND	10	EQ GROUND
11	AC-	12	AC+



FRONT VIEW

MEASURED FROM PC BOARD EDGE TO
CONNECTOR MOUNTING HOLE CENTER

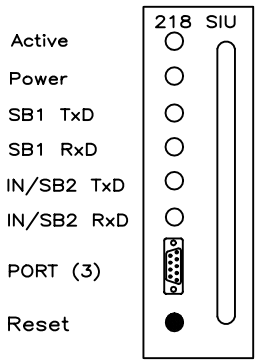


SIDE VIEW

END VIEW

SIU PIN ASSIGNMENTS

PIN	SIU ROW A	SIU ROW B	SIU ROW C
1	+24 VDC in	+24 VDC in	I/O 47
2	I/O 0	1/O 1	I/O 48
3	I/O 2	I/O 3	I/O 49
4	I/O 4	I/O 5	I/O 50
5	I/O 6	I/O 7	I/O 51
6	I/O 8	I/O 9	I/O 52
7	I/O 10	I/O 11	I/O 53
8	I/O 12	I/O 13	SB1 TxD +
9	I/O 14	I/O 15	SB1 TxD −
10	I/O 16	I/O 17	SB1 RxD +
11	I/O 18	I/O 19	SB1 RxD −
12	I/O 20	I/O 21	SB1 TxC +
13	I/O 22	I/O 23	SB1 TxC −
14	I/O 24	I/O 25	SB1 RxC +
15	I/O 26	I/O 27	SB1 RxC −
16	I/O 28	I/O 29	LINE SYNC. +
17	I/O 30	I/O 31	LINE SYNC. −
18	I/O 32	I/O 33	N RESET +
19	I/O 34	I/O 35	N RESET −
20	I/O 36	I/O 37	ASSEMBLY ADDR (*)
21	I/O 38	I/O 39	INBUS RTS
22	I/O 40	I/O 41	SB2 TxD +
23	I/O 42	I/O 43	SB2 TxD −
24	I/O 44	I/O 45	SB2 RxD +
25	I/O 46	Opto Input 1	SB2 RxD −
26	Opto Input 2	Opto Input 3	SB2 TxC +
27	Opto Input 4	Opto Input Ground	SB2 TxC −
28	Address−0	Address−1	SB2 RxC +
29	Address−2	Address−3	SB2 RxC −
30	INBUS TxD	INBUS RxD	INBUS TxC
31	Equipment Ground	AC Line Reference (2)	INBUS RxC
32	24 VDC Ground	24 VDC Ground	SIU/Enable (3)



FRONT VIEW

Port 3 Pin Assignments (DB9S)

1	NA	6	NA
2	RXD	7	NA
3	TXD	8	NA
4	NA	9	NA
5	DC Ground		

NOTES:

1 ○ LED Indicator
● Recessed Momentary Push Button
DB9S Connector
NA Not Applicable
2 NA for ITS Cabinet Standard
3 24VDC Ground for SIU application

TITLE:

MODEL 218 SERIAL INTERFACE UNIT (SIU) DETAILS

NO SCALE

MARCH 29, 2002

3—11—8

CHAPTER 5

SPECIFICATION FOR DETECTOR SENSOR UNITS, ELEMENTS AND ISOLATORS

MODEL 222E TWO-CHANNEL LOOP DETECTOR SENSOR UNIT

MODEL 224E FOUR-CHANNEL LOOP DETECTOR SENSOR UNIT

MODEL 231E MAGNETIC DETECTOR SENSING ELEMENT

MODEL 232E MAGNETIC DETECTOR SENSOR UNIT

MODEL 242 TW0-CHANNEL DC ISOLATOR

MODEL 252 TWO-CHANNEL AC ISOLATOR

TABLE OF CONTENTS

CHAPTER 5 SECTION 1

GENERAL REQUIREMENTS

5.1.1
The sensor and isolator channels shall be operationally independent from each other. Each sensor or isolator channel shall draw no more than 50 mA from the +24 VDC cabinet power supply and shall be insensitive to 700 millivolts RMS ripple on the incoming +24 VDC line.

5.1.2
The sensor unit or isolator front panel shall be provided with the following:

Hand pull to facilitate insertion and removal from the input.
Control switches.
Channel visual indication of detection or incoming signal.

5.1.3
Each sensor or isolator channel output shall be an opto-isolated NPN Open Collector capable of sinking 50 mA at 30 VDC. The output shall be compatible with the controller unit inputs.

5.1.4
A valid channel input shall cause a channel Ground True Output to the controller unit. of a minimum 100 ms in duration. An onboard two-post shunt jumper shall be provided to disallow this requirement when the jumper is in a OPEN position.

5.1.5
The sensor unit or sensing element shall operate and interface successfully with an associate CALTRANS Standard Sensing Unit or Element.

5.1.6
The output transistor shall switch from OFF to ON state or ON to OFF state in 20 µs or less.

5.1.7
Each Enhanced (E) Sensor Unit shall provide a Tri State EIA 423 Serial Port for interface with through pins 19 and 21 of the unit connector to the assembly SIU Connector C03. Each sensor unit shall read in the Slot Address pins located at unit connector for unit slot Identification. Four onboard switches shall match the upper 5th to 8th bits associated Assembly name. Slot Pin 22 shall turn on the SIU Drivers allowing RXD to the ATC. Status and report messages shall meet SDLC Protocol transmitting at 19,200 bps. Said Messages shall be as called out by the user.

5.1.8
Onboard protection shall be provided to enable the sensor unit or isolator to withstand the discharge of a 10 µF capacitor charged to +/- 1000 Volts directly across the input pins with

CHAPTER 5 SECTION 2

MODEL 222E & 224E LOOP DETECTOR SENSOR UNIT REQUIREMENTS

5.2.1
The sensor unit channel shall produce an output signal when a vehicle passes or remains over loop wires embedded in the roadway. The method of detection shall be based upon a design that renders the output signal when a metallic mass (vehicle) enters the detection zone causing a change of 0.02% minimum decrease in inductance of the circuit measured at the input terminals of the sensor unit.

5.2.2
An open, shorted or otherwise malfunctioning loop shall cause the sensor unit channel to output a constant signal state. A two post shunt jumper or approved switch shall be provided to dictate output state upon malfunction. The jumper in closed position (Ground True) shall cause a Ground True Output to the controller unit. An open position (Ground False) shall cause a Ground False Output to the controller unit. An indicator labeled "EOS" (Event Output Status) shall be provided on the front panel. When in closed position, the indicator shall be ON. A second indicator per channel labeled "EVENT" shall be provided indicating a malfunctioning loop or tracking condition. The indicators shall be reset by the Unit RESET Switch.

5.2.3
Each sensor unit channel shall be capable of detecting all types of AGENCY licensed motor vehicles when connected to the loop configuration/lead-in requirements of Heading 5.2.9.1.

5.2.4
The sensor unit shall comply with all performance requirements when connected to an inductance (loop plus lead-in) from 50 to 700 µH with a Q-parameter as low as 5 at the sensor unit operating frequency.

5.2.5
Loop inputs to each channel shall be transformer isolated.

5.2.6
Each individual channel shall have a minimum of 4 switch selectable operating frequencies.

5.2.7
The sensor unit channel tuning circuits shall be automatic and shall be so designed that drift caused by environmental changes or changes in applied power shall not cause an actuation.

5.2.8
Each sensor unit channel shall have PULSE and PRESENCE selectable modes.

5.2.8.1

CHAPTER 5 SECTION 3

MAGNETIC DETECTOR REQUIREMENTS

5.3.1 MODEL 231E MAGNETIC DETECTOR SENSING ELEMENT

5.3.1.1
Each sensing element shall be designed for ease of installation, repositioning, and removal. The sensing element shall be 57 mm maximum in diameter, have no sharp edges, and its length not to exceed 450 mm (18 in). The sensing element shall be constructed of nonferrous material and shall be moisture proof. The element shall contain no moving parts or active components. The element shall have a 15.4 m (50 ft) lead-in cable. Leakage resistance shall be a minimum of 10 megohms when tested with 400 VDC between lead wire, including lead wire entrance, and the fluid of a salt water bath after the device has been entirely immersed in the bath for a period of 24 hours at 20 degrees (+/- 3 degrees) C. The salt water bath concentrate shall be one fourth ounce of salt per gallon of water.

5.3.1.2
Each sensing element including lead-in shall have a DC resistance of less than 3500 ohms and an inductance of 20 Henrys +/- 15 %.

5.3.2 MODEL 232E TWO CHANNEL MAGNETIC DETECTOR SENSING UNIT

5.3.2.1
When resident in a active cabinet input assembly and attached to one or more Model 231E Sensing Elements resident in conduit under the travelway, the sensing channel shall output a Ground True Output to the Controller Unit when sensing an induced voltage caused by a California Licensed Vehicle passing within 1.83 M from an element with a 305 M of lead-in cable at all speeds between 5 and 130 KMPH. The sensing channel output shall be continuous as long as the vehicle is detected. A digital reading switch with 8 selected step positions for Gain (O to Full) and a momentary test switch providing a voltage test input shall be furnished for each channel on the front panel.

In the PULSE MODE, each new vehicle presence within the detection zone shall initiate a sensor unit channel output pulse of 125 (+/- 25) ms in duration. Should a vehicle remain in a portion of the detection zone for a period in excess of 2 seconds, the sensor unit channel shall automatically "tune out" the presence of said vehicle. The sensor unit channel shall then be capable of detecting another vehicle entering the same detection zone. The recovery time to full sensitivity between the first vehicle pulse and channel capability to detect another vehicle shall be 3 seconds maximum.

5.2.8.2
In the PRESENCE MODE, the sensor unit channel shall recover to normal sensitivity within 1 second after termination of vehicle presence in the detection zone regardless of the duration of the presence. The channel sensitivity settings 2 & 6 shall provide presence detection of a vehicle in the detection zone for a specified time period and inductance change(s). The conditions are as follows:

	MINIMUM TIME DURATION IN MINUTES	DETECTOR INPUT INDUCTANCE CHANGE
SETTING 6	3 10	0.02% or more 0.06% or more
SETTING 2	4	1.00% or more

5.2.9
Sensitivity

5.2.9.1
California Standard Plan ES-5A & B Loop Configurations. (California Department of Transportation Standard Plans.)

5.2.9.1.1
Single Type A, B, Q or Round Loop with a 250 foot lead-in cable.

5.2.9.1.2
Single Type A, B, Q or Round Loop with a 1000 foot lead-in cable.

5.2.9.1.3
4 Type A, B, or Q Loops connected in series/parallel with a 250 foot lead-in cable.

5.2.9.1.4
4 Type A, B, Q or Round Loops connected in series with a 1000 foot lead-in cable.

5.2.9.1.5
One 50 foot Type C Loop with a 250 foot lead-in cable.

5.2.9.2
Each sensor unit channel shall be equipped with 7 selectable (digitally read) sensitivity setting(s) in presence and pulse modes to accomplish the following under operational and environmental requirements of this specification:

SETTING	SESITIVITY	SETTING	SENSITIVITY
1	0.64 % delta L	5	0.04 % delta L
2	0.32 % delta L	6	0.02 % delta L
3	0.16 % delta L	7	0.01 % delta L
4	0.08 % delta L	0	Channel OFF

5.2.9.2.1
All sensitivity settings shall not differ +/- 40% from the nominal value chosen.

5.2.9.3
Each sensor unit channel shall not detect vehicles, moving or stopped, at distances of 3 feet or more from any loop perimeter, in all configurations listed in paragraph 5.2.9.1.

5.2.10
Response time of the sensor unit channel for Sensitivity Settings 1, 2 & 3 shall be less than 5 +/- 1 ms at an approximate loop frequency of 40 KHZ. That is, for any decreased inductive change which exceeds its sensitivity threshold, the channel shall output a ground true logic level within 5 +/- 1 ms. When such change is removed, the output shall become an open circuit within 5 +/- 1 ms.

5.2.11
The sensor unit channels shall begin normal operation within 2 seconds after the application of power or after a reset signal of 30 µs.

5.2.12
Tracking Rate – The sensor unit shall be capable of compensating or tracking for an environmental change up to 0.001% change in inductance per second.

5.2.13
Tracking Range - The sensor unit shall be capable of normal operation as the input inductance is changed from +/- 5.0% from the quiescent tuning point regardless of internal circuit drift. The sensor unit shall be capable of normal operation as the input resistance is changed from +/- 0.5% from the quiescent tuning point regardless of internal circuit drift.

5.2.14
Temperature Change – The operation of the sensor unit shall not be affected by changes in the inductance and/or capacitance of the loop caused by environmental changes with the rate of temperature change not exceeding 1 degree C per 3 minutes. The opening or closing of the controller cabinet door with a temperature differential of up to 18 degrees C between the inside and outside air shall not affect the proper operation of the sensor unit.

no load present. With a dummy load of 5 Ohms, protection shall enable the sensor unit or isolator to withstand the discharge of a 10 µF capacitor charged to +/- 2000 Volts directly across either the input pins or from either side to equipment ground.

CHAPTER 5 SECTION 4

MODEL 242 TWO-CHANNEL DC ISOLATOR REQUIREMENTS

5.4.1
The Model 242 DC Isolator Channel shall provide isolation between a VDC input circuit (external electrical switch closure) and the controller unit input. The minimum isolation shall be 1000 Megohms and 2,500 VDC measured between the input and the output of the same channel.

5.4.2
Each isolation channel shall have a front panel mounted test switch to simulate valid input. The test switch shall be a single-pole double-throw, three position CONTROL test switch: The position assignment shall be UP – constant ON; MIDDLE – OFF; and DOWN – momentary ON.

5.4.3
The isolator shall have an internal power supply supplying 20 +/- 4 VDC to the field input side of the isolation channels. The isolator shall not draw more than 2.5 watts of AC power. No current shall be drawn from the cabinet power supply.

5.4.4
A channel contact closure input of 2 ms or less shall not cause an output (ground true) to the controller. An input of 7 ms or greater shall cause an output to the controller. An input of duration between 2 and 7 ms may or may not cause an output to the controller. .

5.4.5
Each isolation channel field input shall be turned on (true) when a contact closure causes an input voltage of less than 8 VDC, and shall be turned off (false) when the contact opening causes the input voltage to exceed 12 VDC. Each input shall deliver no less than 15 mA nor more than 40 mA to an electrical contact closure or short from the power supply.

CHAPTER 5 SECTION 5

MODEL 252 TWO-CHANNEL AC ISOLATOR

5.5.1
The Model 252 Two-Channel AC Isolator shall contain 2 isolation channels which provide isolation between external 120 VAC input circuits and the controller unit input circuits. The method of isolation shall be based upon a design which provides reliable operation.

5.5.2
A channel input voltage "Von" of 80 +/- 5 VAC applied for a minimum duration of 110 ms ± 10 ms shall cause an output (Ground True) to the controller unit.

5.5.3
A channel input voltage "Voff" (Von minus 10 VAC) applied for a minimum duration of 110 ms ± 10ms shall cause an output (Ground False) to the controller unit.

5.5.4
A two post jumper shall be provided to select inverted output states for Von and Voff. When in CLOSED position (Grounded) Von shall cause a Ground False output. An indicator shall be provided on the front panel labeled 'RR" which shall indicate a Voff input, Ground True output.

5.5.5
The input impedance of each channel shall be between 6,000 - 15,000 Ohms at 60 Hz.

5.5.6
The minimum isolation shall be 1000 Megohms between the input and output terminals at 500 AC applied voltage.

CHAPTER 7

SPECIFICATION FOR ITS CABINET

TABLE OF CONTENTS

CHAPTER 7 - SECTION 1

CABINET SYSTEM REQUIREMENTS

7.1.1 GENERAL

7.1.1.1
The Intelligent Transportation System (ITS) Serial Interconnected Cabinet Family is a group of cabinets designed to fulfill a variety of applications (26 have been identified). This specification describes the functional and physical requirements of said cabinets.

7.1.1.2
There are common parts to all cabinets such as Housing, Cage(s), Modular Bus and Power Assemblies, Electronic Communications Terminal Assembly (ECTA), Cabinet Emergency Override System, harnesses and Advanced Transportation Controller (ATC). The Power Distribution Assembly (PDA ITS), Input and Output Assemblies used and their plug in Units shall depend upon application need.

7.1.1.3
The ATC Controller shall be here in referred to as the Model 2070 Controller Unit. The 2070 Unit is serially connected to the Cabinet via its two serial synchronous ports located at the C12 Connector. These two communication links use EIA-485 Drivers/Receivers and Synchronous Data Link Control (SDLC) Protocol to interface with Serial Bus #1 and #2.

7.1.1.4
The Stop Time, Manual Advance and manual Control Enable switches are not required unless called out in the Agency Contract Special Provisions. The Cabinets shall be wired for these features.

7.1.2 CABINET MODEL NUMBER AND CONSISTENCY

7.1.2.1
The ITS Cabinets shall consist of a package of items needed to carry out the specific Application. The Cabinet VERSION Package List is as follows:

Cabinet Traffic Signal Application - Series 340
- **340 - 4 Door Cabinet with "P" Base Ground Mount**
- **342 - 2 Door Cabinet with "170" Base Ground Mount**
- **346 - 2 Door Cabinet with "170" Base, Adaptor Mount**

Cabinet Traffic Management Application - Series 350
- **354 - 2 Door Cabinet with "170" Base Ground Mount**
- **356 - 2 Door Cabinet with "170" Base Adaptor Mount**

	Versions				
Package Items	**340**	**342**	**346**	**354**	**356**
Housing #1 / Cage #1	**-**	**1**	**-**	**1**	**-**
Housing #2 / Cage#2	**-**	**-**	**1**	**-**	**1**
Housing #3 / Two Cage #1	**1**	**-**	**-**	**-**	**-**
"J" Panel Cage #1	**4**	**2**	**-**	**2**	**-**
"J" Panel Cage #2	**-**	**-**	**2**	**-**	**2**
Service Panel Assembly w/ AC-/EG Bus	**1**	**1**	**1**	**1**	**1**
AC Power Extension	**1**	**-**	**-**	**-**	**-**
Clean / Raw AC Power Assembly	**1**	**1**	**1**	**1**	**1**
DC Power / COMM Assembly	**2**	**1**	**1**	**1**	**-**
Cage Shelf Assembly	**1**	**1**	**1**	**1**	**1**
Input Assembly	**3**	**2**	**1**	**1**	**1**
Six Pack Output Assembly	**1**	**-**	**-**	**1**	**1**
Fourteen Pack Output Assembly	**1**	**1**	**1**	**-**	**-**
PDA ITS Assembly	**1**	**1**	**1**	**1**	**1**
Control / Serial Bus Harness	**8**	**6**	**4**	**4**	**4**
Serial Bus 3 Harness	**3**	**1**	**1**	**1**	**1**

Note: Input Assembly includes a Model 218 SIU. Output Assembly includes a Model 218 SIU, Model 214 AMU and Flash Transfer relays. The PDA ITS (Traffic Signal Application) includes two Model 204 Flasher Units, Model 212 CMU and two Model 216 Power Supply Units. The PDA ITS (Traffic Management System Application) includes Model 212 CMU and two Model 216 Power Supplies.

7.1.3 SERIAL BUS # 1 SYSTEM

7.1.3.1

Serial Bus #1 functions as the real-time cabinet control and communications. The Bus Commands are generated in the ATC Controller Unit. They are passed to the assembly Model 218 SIU Units and Model 212 CMU Monitor Unit using EIA 485 COMM/SDLC Protocol Frame Address/Message Packets. The Units read the Four lines Assembly Molex Connector for Assembly Address Number and compares it to the SDLC Address Frame.

7.1.3.2

The following Address Frame numbers are assigned to the assemblies and monitor as:

14 Pack Output Assembly Pos #1	**01**	**0000**	**0001**
14 Pack Output Assembly Pos #3	**03**	**0000**	**0011**
06 Pack Output Assembly Pos #1	**05**	**0000**	**0101**
06 Pack Output Assembly Pos #2	**06**	**0000**	**0110**
06 Pack Output Assembly Pos #3	**07**	**0000**	**0111**
06 Pack Output Assembly Pos #4	**04**	**0000**	**0100**
Input Assembly #1	**09**	**0000**	**1001**
Input Assembly #2	**10**	**0000**	**1010**
Input Assembly #3	**11**	**0000**	**1011**
Input Assembly #4	**12**	**0000**	**1100**
Input Assembly #5	**13**	**0000**	**1101**
Cab Monitor Unit	**15**	**0000**	**1111**

If the Command Address Frame matches the Unit, the Unit reads in the message for processing and response. The Message First Byte is the message name. The Unit responses by setting the SDLC Address Frame to "19" or CPU of the ATC. The Unit sets the Response Packet First Byte to Command Message plus 127 and the appropriate data. The Command / Response required Buffers, Drivers and Messages are listed in Chapter 9, Sections 2 and 3; and Chapter 3, Sections 7, 8 and 10.

7.1.4 SERIAL BUS #2 SYSTEM

7.1.4.1

Serial Bus #2 is dedicated to gathering preprocessed data from the Cabinet Enhanced Detectors resident in the input assemblies. This serial bus shall be off- line use in operation with the ATC controlling data collection. The Serial Bus #2 is designed to operate Synchronous or Asynchronous 485 lines at selected bps up to 1 Mega-BPS. See Chapter 3 Section 10 SIU Unit requirements for communication, interface and message protocol.

7.1.4.2

The next generation input assembly is planned to use DIN 64 or 96 Pin Connectors allowing a better non legacy addressing scheme for "Smart Devices". "Smart Devices" are defined as Advanced Detector and Output Units capable of direct serial communications with the ATC Controller Unit. Synchronous serial port 3 of the ATC CPU is assigned to the Bus and functions as COMMAND linkage to the system.

7.1.4.3

Typical Command/Response Messages shall use the same message format as Serial Bus #1 collecting Operational Status. Detection Speed reports, Occupancy reports, Counts and etc.

7.1.5 CABINET EMERGENCY OVERRIDE SYSTEM (CEOS)

7.1.5.1
SYSTEM DESCRIPTION

The Emergency System is composed of the Police Panel Switches, Door Switches, Power Distribution Assembly ITS with resident Cabinet Monitor Unit, Serial Bus #1, AC Modular Assembly and cable/s, and the Output Assemblies with Transfer Relays and Program Block Connectors. The purpose of this system is to transfer control from the ATC to the EMERGENCY OVERRIDE SYSTEM Control when called for by the Cabinet Monitoring System or Manual Action. The action taken depends upon the application. The concluding act is switching the Transfer Relays in the Output Assemblies from Switch Pack Control to the CEOS control including power turn off via the system Main Contactor. The result for Traffic signal Control is Intersection is FLASH Mode and the Ramp Metering application is NO INDICATION or BLANK Mode.

7.1.5.2
SYSTEM MONITORING SYSTEM

The Cabinet Monitoring System is composed of Serial Bus #1, the Control / Serial Bus Harnesses, the DC Power/COMM Assembly, the 212 Cabinet Monitor Unit with application DATAKEY resident in the PDA ITS, Serial Bus #3 Harnesses interconnecting the output assemblies to the monitor (if required) and the 214 Auxiliary Monitor Unit(s) resident in all other output assemblies. See Chapter 3 Sections 7 and 8 (CMU and AMU) for operations, functions, protocol, Message frames and bit rate.

Serial Bus #3 System – Serial Bus #3 is composed of the Model 212 Cabinet Monitor Unit (CMU) resident in the PDA ITS, the Bus Harnesses daisy chained between the Output Assemblies and the PDA ITS and the Model 214 Auxiliary Monitor Units (AMU) resident in the Assemblies. The Model 212 Monitor shall originate the Commands and the Auxiliary Monitor Unit(s) the Responses. See AMU specifications for Serial Bus #3 Requirements.

CHAPTER 7 - SECTION 2

HOUSINGS

7.2.1
HOUSING PACKAGE - The housings shall include, but not be limited to, the following:

Enclosure & Doors	**Gasketing**	**Lifting Eyes & External Bolt Heads**
Door Latches & Locks	**Ventilation**	**Cage Supports & Mounting**
Door Hinges & Catches	**Police Panel**	**Aluminum Surfaces**

7.2.2
HOUSING CONSTRUCTION - The housing shall be rainproof. It shall have front and rear doors, each equipped with a lock and handle. The enclosure top shall be crowned to prevent standing water. The aluminum surface shall be either coated with an Anodic Coating or Anti-graffiti Paint.

7.2.2.1
MATERIAL THICKNESS - The enclosure, doors, lifting eyes, gasket channels, police panel door, spacer supports and all supports welded to the enclosure and doors shall be fabricated of 3.175mm (0.125 inch) minimum thickness aluminum sheet. The filter shell, filter trough, fan support and police panel enclosure shall be fabricated of 2.032mm (0.080 inch) minimum thickness aluminum sheet. The spacer supports shall have the option to use 0.15mm (0.059 inch) minimum stainless steel sheet.

7.2.2.2
WELDS - All exterior seams for enclosure and doors shall be continuously welded and shall be smooth. All edges shall be filled to a radius of 0.794mm (0.03125 inch) minimum. Exterior cabinet welds shall be done by gas Tungsten arc TIG process only. ER5356 aluminum alloy bare welding electrodes conforming to AWS A5.10 requirements shall be used for welding on aluminum. Procedures, welders and welding operators shall conform to the requirements and practices in AWS B3.0 and C5.6 for aluminum. Internal cabinet welds shall be done by gas metal arc MIG or gas Tungsten arc TIG Process.

7.2.2.3
ALUMINUM SURFACE PROTECTION shall be either ANODIC or ANTI-GRAFFITI Paint.

7.2.2.3.1

ANODIC COATING - An anodic coating shall be applied to the aluminum surface after the surface has been cleaned and etched. The cleaning and etching procedure shall be to immerse in inhabited alkaline cleaner at 71°C for five minutes (Oakite 61A, Diversey 909 or equivalent in mix of the 6 to 8 ounces per gallon to distilled water). Rinse in cold water. Etch in a sodium solution at 66°C for 5 minutes 90.5 ounce sodium fluoride plus 5 ounces of sodium hydroxide mix per gallon to distilled water. Rinse in cold water. Desmut in a 50% by volume nitric acid solution at 20°C for 2 minutes. Rinse in cold water. The anodic coating shall conform to MIL-A-8625C (Anodic Coatings for Aluminum and Aluminum Alloys) for Type II, class I Coating except the outer housing surface coating shall have a 0.01778mm minimum thickness and a 0.04186 milligrams per square mm minimum coating weight. The anodic coating shall be sealed in a 5% aqueous solution of nickel acetate 4 (pH 5.0 to 6.5) for 15 minutes at 99°C.

7.2.2.3.2

ANTI – GRAFFITI PAINT – The aluminum surface shall be cleaned, etched and rinsed per above anodic coating requirements. Dry surfaces by preheating in an oven for 15 minutes at 400 degrees F. Remove and coat the surfaces using TCI Wheel Silver # 9811-0110 with a minimum film build of not more than 2 mils total thickness. Place back into preheated oven for 10 minutes minimum at 360 degrees F to gel the base coat. Remove and coat the surfaces using TCI Anti-graffiti Clear # 9810-0231. Place back into oven and fully cure at 380 degrees F for 40 minutes.

7.2.2.4

Enclosure Door Frames and door seals - The enclosure door frames shall be double flanged out on all 4 sides and shall have strikers to hold tension on and form a firm seal between the door gasketing and the frame. The dimension between the door edge and the enclosure external surface when the door is closed and locked shall be 3.9624 (±2.032) mm (0.156 inch).

7.2.3

GASKETING - Gasketing shall be provided on all door openings and shall be dust-tight. Gaskets shall be 6.35mm minimum thickness closed cell neoprene or silicone (BOYD R-108480 or equal) and shall be permanently bonded to the metal. A gasket top channel shall be provided to support the top gasket on the door to prevent gasket gravitational fatigue.

7.2.4

CAGE MOUNTING SUPPORTS - Cage mounting supports shall be provided on either side, level with the bottom edge of the door opening, for horizontal support and bolt attachment; side cage supports provided for the bracket cage supports; and bracket cage support attachments.

7.2.5

LIFTING EYES and EXTERIOR BOLT HEADS - The housing shall be provided with 2 lifting eyes for placing the cabinet on its foundation. Each eye opening shall have a minimum diameter of 19.05mm (0.75 inch). Each eye shall be able to support the weight load of 450 Grams (1.000 lbs). All bolt heads shall be tamperproof type.

7.2.6

DOOR LATCHES AND LOCKS - The latching handles shall have provision for padlocking in the closed position. Each handle shall be 19.05mm (0.75 inch) minimum diameter stainless steel with a minimum of 12.7mm (0.50 inch) shank. The padlocking attachment shall be placed at 101.6mm (4 inch) from the handle shank center to clear the lock and key. An additional 101.6mm (4 inch) minimum gripping length shall be provided.

7.2.6.1

Latch/ Lock Mechanism - The latching mechanism shall be a three-point draw roller type. The pushrods shall be turned edgewise at the outward supports and have a cross section of 6.35mm (0.25 inch) thick by 19.05mm (0.75 inch) wide minimum. Rollers shall have a minimum diameter of 22.225mm (0.875 inch) with nylon wheels and steel ball bearings. When the door is closed and latched, the door shall be locked. The lock and lock support shall be rigidly mounted on the door. In the locked position, the bolt throw shall extend a minimum of 6.35 ± 7.9375mm (0.25 ± .03125 inch) into the latch Cam area. A seal shall be provided to prevent dust or water entry through the lock opening.

7.2.6.2

Locks & Keys - The locks shall be Corbin 2 type. One key shall be supplied with each lock. The keys shall be removable in the locked position only. The locks shall have rectangular, spacing loaded bolts. The bolt shall have a 7.1374mm (0.281 inch) throw and shall be 19.05 mm (0.75 inch) wide by 9.525mm (0.375 inch) thick. Tolerance is ±0.899mm (0.035 inch).

7.2.6.3

Cam - The center latch cam shall be fabricated of a minimum thickness 4.7625mm aluminum. The bolt surface shall horizontally cover the cam thickness. The cam shall be structured to only allow the door to open when the handle is moved toward the center of the door.

7.2.7

HOUSING VENTILATION - Shall including intake, exhaust, filtration, and continuous running fan assembly.

7.2.7.1

Intake & Filter - The louvered vent depth shall be a maximum of 6.35 mm (0.25 inch). A removable and reusable air filter shall be housed behind the door vents. The filter filtration area shall cover the vent opening area. A filter shell shall be provided that fits over the filter providing mechanical support for the filter. The shell shall be louvered to direct the incoming air downward. The shell sides and top shall be bent over a minimum of 6.35mm (0.25 inch) to house the filter. The filter resident in its shell shall be held firmly in place with a bottom trough and spring loaded upper clamp. No incoming air shall bypass the filter. The bottom filter trough shall be formed into a waterproof sump with drain holes to the outside housing. The filter shall be 406.4 mm (16 inch) wide by 304.8 mm (12 inch) high by 22.225 mm (0.875) thick. The filter shall be an ECO-AIR Product E35S or equal. The intake (including filter with shell) and exhaust areas shall pass a minimum of 60 cubic feet of air per minute for Housing #1; 120 cubic feet of air per minute for Housing #3; and 26 cubic feet of air per minute for Housing #2.

7.2.7.2

Fan - Each electric fan shall be equipped with ball or roller bearings and with a capacity of at least 100 cubic feet of free air delivery per minute. The fan shall be mounted within the housing and vented.

7.2.8

HINGES AND DOOR CATCHES – hinges (Two-bolts per leaf) shall be provided to bolt the enclosure to the doors. Housing #1 & Housing #3 shall have four hinges per door and Housing #2 shall have three hinges per door. Each hinge shall be 88.9mm (3.5 inch) minimum length and have a fixed pin. The pin ends shall be welded to hinge and ground smooth. The pins and bolts shall be covered by the door edge and not accessible when the door is closed.

7.2.9

DOOR CATCHES - Front and rear doors shall be provided with catches to hold the door open at both 90 and 165 ± 10 degrees. The catch minimum diameter shall be 9.525mm (0.375 inch) aluminum rods. The catches shall be capable of holding the door open at 90 degrees in a 60 mph wind acting at an angle perpendicular to the plane of the door.

7.2.10

POLICE PANEL - A police panel assembly shall be provided to allow the police officers limited control access. The panel door shall be equipped with a lock and master police key. The front and back of the panel shall be enclosed with a rigid metal covering so that no parts having line voltage are exposed. The panel assembly shall have a drain to prevent water from collecting within the assembly. The drain shall be channeled to the outside. The series 35X Cabinets shall have one switch provided and labeled "ON - OFF LIGHTS". The series 34X Cabinets shall have one switch labeled "ON - OFF" and the other "FLASH/AUTOMATIC".

CHAPTER 7 SECTION 3

CABINET CAGES

7.3.1
A standard EIA 19-inch (482.6mm) Rack Cage shall be installed inside the housing for mounting of the controller unit and cabinet assemblies. The EIA rack portion of the cage shall consist of 2 Pairs of continuous, adjustable equipment mounting angles. The angle nominal thickness shall be either 3.4163mm (0.1345 inch) plated steel or 2.667mm (0.105 inch) stainless steel. The angles shall be tapped with 10-32 threads with EIA universal spacing. The angle shall comply with standard EIA-310-B and shall be supported at the top and bottom by either welded or bolted support angles to form a cage.

7.3.2
Clearance between rails for mounting assemblies shall be 450.85mm (17.75 inch).

7.3.3
The cage shall be bolted to the cabinet at 4 points via the housing cage supports and 4 points via associated spacer brackets (top and bottom).

7.3.4
The cage(s) shall be centered within the cabinet.

CHAPTER 7 - SECTION 4

CABINET ASSEMBLIES

7.4.1
GENERAL

7.4.1.1
Cabinet Assemblies - The cabinet assemblies shall be completely removable and installable from the cabinet cage without removing any other equipment and using only a Standard Slotted or Phillips Screwdriver.

7.4.1.2
Visible & Accessible Devices - All fuses, circuit breakers, switches (except Police Panel Switches and Fan Fuse) and indicators shall be readily visible and accessible when the cabinet front door is open.

7.4.1.3
Labels & Marker Strips - All equipment in the cabinet, when required shall be clearly and permanently labeled. The marker strips shall be made of material that can be easily and legibly written on using a pencil or ballpoint pen. Marker strips shall be located immediately below the item they are to identify and must be clearly visible with the items installed.

7.4.1.4
Resistor / Capacitor Suppression – Suppression shall be provided at all relay sockets (across relay coil) except for the Flash Transfer Relays (FTR) in the output assemblies where one suppression device may be common for all.

7.4.1.5
Assembly Width and Depth Dimension – the Assembly Depth shall include terminal sockets, plug-in units and strain relief bar. The Width shall be 17.5 Maximum. Including side screws.

7.4.1.6
Assembly Housing - The assembly housing top and bottom shall be slotted for vertical ventilation. Assembly Thickness - Side ends shall be fabricated of 0.0203mm (0.080 inch) minimum thickness aluminum sheet. All other surfaces shall be fabricated of 0.015875mm (0.0625 inch) minimum thickness aluminum sheet. The aluminum metal surface shall be treated with clear chromate.

7.4.1.7
Connector Sockets - Flasher and Switchpack Unit sockets shall be mounted with their front face 190.5mm (7.50 inch) from the assembly front panel.

7.4.1.8
Nylon Guides - Guides (top and bottom) shall be provided for assembly Plug-in units (Power Supply Units guide on bottom only). The guides shall begin 12.7mm (0.50 inch) from the assembly front panel face.

7.4.2
"J" PANEL ASSEMBLIES The J Panels shall be mirror images of each other when mounted in the cabinet cage. They shall be bolted to the cage with the matching shelve unit bolted to the panel.

7.4.3
CABINET SHELF ASSEMBLIES A Shelve Assembly shall be provided unless otherwise called out in the contract special provisions.

7.4.4
SERVICE PANEL ASSEMBLY

7.4.4.1
A Service Panel Assembly shall be provided. The assembly shall function as the entry point for AC Power to the cabinet; cabinet protection and power filtering / transient suppression; AC- & Equipment Ground Bussing and both Raw and Clean AC Power Source.

7.4.4.2
Location - The assembly shall be located on the lower right J Panel when viewed from the back door.

7.4.4.3
Service Terminal Block – The terminals of the STB shall be labeled L1, L2 and EG and shall be covered with a clear insulating material to prevent inadvertent contact. The Terminating Lugs shall be large enough to accommodate # 2 conductors.

7.4.4.4
AC+ Raw, AC- Raw & Equipment Ground Buses – A Post for AC+ Raw and Two 10 position minimum AC- Raw & Equipment Ground Copper Bus Bars shall be provided on the right J Panel viewed from the rear door.

7.4.5
RAW/CLEAN AC POWER ASSEMBLY This Assembly shall be provided in all Versions. It shall provide Six Clean AC Power Receptacles for assemblies and cabinet units; Raw AC Power to the Output Assemblies; and both logic and power to the ventilation system, door opening circuitry and logic interface (all via CC1 and 2 Connectors).

7.4.5.1
R/C AC Power Extension - The Extension shall provide a minimum of five additional NEMA 5-15 receptacles with harness plug connector for plugging into the main assembly.

The extension is available as an option in Housing #1 and #2 and required in Cage 2 of the Housing #3.

7.4.6
DC POWER/COMMUNICATIONS ASSEMBLY - The Assembly shall be provided in all versions. It shall function as the DC Power bus providing Six VDC BEAU S5404-SB Receptacles; ATC System Logic Lines (Power Down, NRESET and LINESYNC) and Seven System Serial Bus DB-25S Connectors (Serial Bus Interfaces).

7.4.6.1
DC/ COMM Extension - The Extension provides additional Serial Bus Connectors and DC Receptacles. This is provided as an option where needed per application.

7.4.7
POWER DISTRIBUTION ASSEMBLY ITS
The Power Distribution Assembly ITS is 19-inch rack mounted assembly that provides for protection and distribution of AC power and production of DC power and distribution. The PDA ITS provides residence for the Cabinet Monitor Unit (CMU) and logic control circuits including a Main Contactor (MC) for control of the load circuits. The PDA ITS contains the required amount field circuits determined by the application; Maintenance circuitry with protection circuit breaker and GFI equipment receptacles; and a ganged 20 Ampere flasher protection/ flasher units if determined by application.

7.4.7.1
The Application shall determine the amount of modules and units supplied. If the PDA ITS is used in a 34X Series, the amount of load circuit breakers shall be eight and two model 204 flasher units with ganged CB Protection Shall be provided. If the PDA ITS is used in the series 35X, four field load circuit breakers are required and no Flasher Units with ganged circuit breaker protection. DC Power generation shall be done by the two provided Model 216 (+12 Volt and +24 Volt) Power Supply units.

7.4.7.2
The Load Circuit Breakers shall have auxiliary internal switches. The auxiliary switches shall indicate by closure that the load breaker has tripped and will transfer the power from the Main Contactor to Flash/ blank

7.4.7.3
Rating of breakers shall be shown on the face of the breaker or handle. Breaker function shall be labeled below the breakers on the front panel.

7.4.7.4
The maintenance equipment circuit shall include a 15-Ampere Circuit Breaker and receptacles on both the front and back of the assembly. The back receptacle shall be the first with GFI Protection defined in the National Electrical Code. Circuit interruption shall occur on 6ma of ground fault-current and shall not occur less than 4ma of ground-fault current.

7.4.7.5
The AUTO/FLASH Switch when placed in FLASH position (down) shall deenergize the Main Contactor (MC) coil and energize the Transfer Relays (TR's) When the switch is placed in the AUTO position (up) the MC Coil shall be energized able the Transfer Relays shall be de energized. The switch shall be a DPST Control Switch.

7.4.7.6
The DC Power shall be brought out to the back panel BEAU S5404-SB Receptacle. A 18 inches minimum DC Power (DCP) Harness of 3#18 cable with a BEAU P5404-LAB Connector on each end shall be provided. The harness shall be plugged in to the PDA ITS power receptacle and the DC / COMM Assembly.

7.4.7.7
A AC Power terminal shall be provided on the back of the assembly for incoming AC Raw Power. A minimum 18 inches AC Power (ACP) Harness of 3#18 cable shall be routed between the Service Panel Assembly and the PDA ITS terminal. The PDA ITS Assembly shall have a resident ACP Harness with assembly strain relief and the other end a BEAU P5412-DB and CC Connectors mating to the Raw/Clean AC Power Assembly.

7.4.7.8
Ganged Circuit Breakers shall be assembled by the circuit breaker manufacturer and certified that their circuit breakers shall gang trip.

7.4.8
INPUT ASSEMBLY

7.4.8.1
The Input Assembly shall be an EIA 19-inch rack mounted assembly providing 12 slots of 22/44 pin PCB sockets. A Model 218 Serial Interface Unit (SIU) shall be provided in its location mated to a DIN 96-pin connector. The SIU shall provide interface and control between the ATC Controller and the input units via System Serial Bus #1 and #2. (SEE CHAPTER 3, SECTION 10 Model 218 SIU for System Operation and Interface).

7.4.8.2
The present input assembly is wired to accept Model 222 (E) and 224 ILD Sensor Units, Model 232E Magnetic Sensor Unit, Model 242 and 252 Isolator Units and Slot mounted NEMA Detectors. Each slot connector is a PCB 22/44 Pin Socket type wired for 2 and 4 channels. The F and W Unit Output pins provide the 24 Inputs to the SIU Channel 1 (Serial Bus #1). In addition, NEMA Status inputs are provided on pins 7 and 20. INBUS is provided on pin 19 and 21 with four slots address lines matching NEMA pin outs.

7.4.8.3
The SIU Unit provides 6 detector RESET Outputs, one for every two slots and should the NEMA Status not be required a RESTART Output from the SIU to the sensor units as a soft reset per channel.

7.4.8.4
The INBUS interfaces with the SIU Channel 2 to provide communications between "Smart Input Units" and Serial Bus #2. The SIU functions as a go between for the ATC and Input Units (no processing).

7.4.8.5
A 25 Pin DB Connector shall be provided on the left assembly side to interface the assembly (SIU) to the DC/COMM Assembly Serial Bus #1 and #2.

7.4.8.6
Four special function Inputs shall be provided via DB-9 CDC Connector to the SIU.

7.4.8.7
The assembly height shall be 5.25 inches (3 U).

7.4.8.8
A harness cable terminated with a BEAU S5404-SB connector shall be supplied for interconnect of DC +24/+12V power.

7.4.8.9
Pins D, E, J, K, and L on each PCB Connector slot shall be routed to their associated field terminal.

7.4.8.10
Each Input Assembly shall contain a 4-bit address code plug and socket. The Input Assembly address shall be provided by a plug with jumpers installed to produce a binary code 1, 2, 4, and 8. The address receptacle shall be installed on the back panel of the Input Assembly, Ground True Logic shall be used with Ground True equaling Logic "1".

7.4.9
OUTPUT ASSEMBLY

7.4.9.1
The Output Assembly shall be an EIA 19-inch rack mounted assembly delivered in 6 Switchpack or 14 Switchpack configuration. This assembly provides capability dependent on configuration the capability of 18 load circuits and 42 load circuits. Either configuration is designed to interface with a plug in Model 200 Switchpack Unit. The SIU shall be provided resident in its connector to provide interface and control. In addition a Model 214 AMU Unit shall be provided in its connector to sense voltage and current for the CMU.

7.4.9.2
Three Model 205 relay units and six Program Blocks shall be provided to select control and color state of the emergence state (red, yellow or no indication output). The programming

connectors shall be Molex Type 1375 or equal. The Units and blocks shall be mounted on the rear of the Output Assembly. Plug Pins shall be crimped and soldered. The Model 205 transfer relays shall be accessible on the rear of the Output Assembly without the use of tools or removal of any other equipment.

7.4.9.3
An Address Plug and Socket shall be provided on Output Assembly for defining the Serial Bus #1 location and addressing. See Model 218 SIU Unit specification and details.

7.4.9.4
Torroids shall be provided the incoming AC current for each Switchpack. See Chapter 3 Model 214 AMU specification.

7.4.9.5
Field Termination shall be provided on the rear panel of the assembly consisting of six position sockets and plugs

7.4.9.6
Transient suppression shall be provided on rear panel of the assembly consist of three nine position sockets and plugs. Each socket shall provided protection for two Switchpacks.

7.4.9.7
A Serial Bus #1 (SB1/SB2) DB25 female connector shall be provided on the upper left rear panel of the Output Assembly for serial interconnection to the DC Communication Bus #l.

7.4.9.8
A CDC Connector shall be provided on the rear panel of the Output Assembly for signal interconnection to the unit.

7.4.9.9
Two RJ-11S Connectors shall be provided on the rear panel of the Output Assembly for signal interconnection of Serial Bus #3.

7.4.9.10
An Equipment Ground Lug shall be provided on the rear panel for termination of a #8 green wire.

7.4.9.11
The 6-Pack assembly height shall be 5.25 inches (3 U) and the 14-Pack shall be 10.5 inches.

7.4.10
CABINET HARNESSES: Cabinet Harnesses are supplied with each cabinet configuration. See Serial Bus and DCP Harness Details.

7.4.11

EXTERNAL COMMUNICATIONS TERMINATION ASSEMBLY This assembly requirements have not yet been defined, In the near future there will be need for Copper / Fiber external interface.

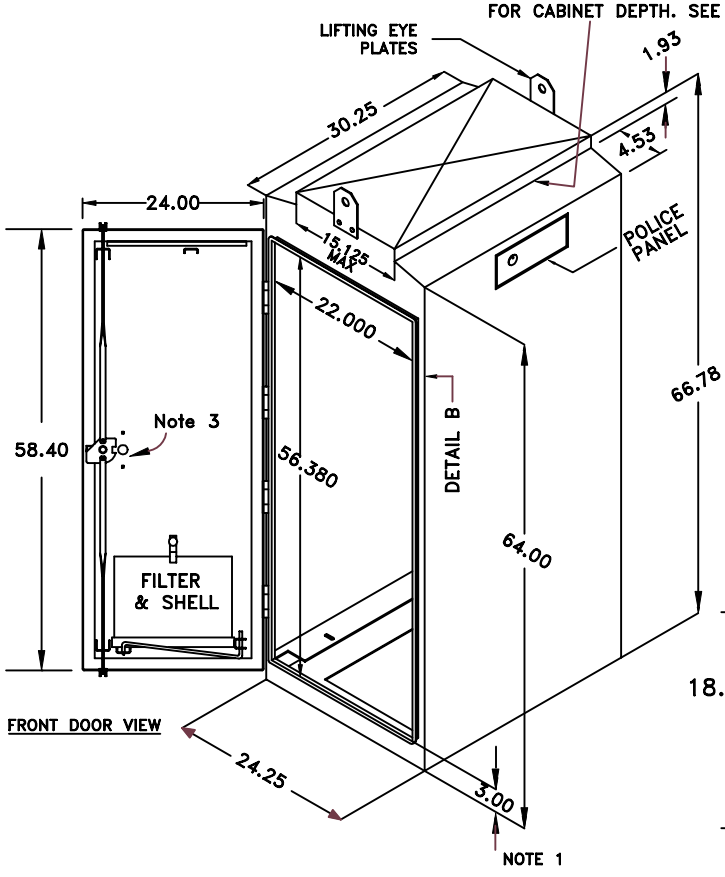
CHAPTER 7 SECTION 5

CABINET DETAILS

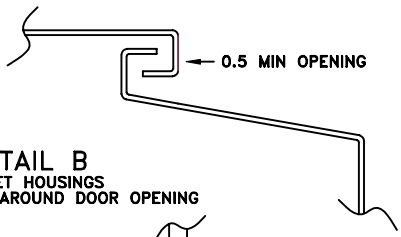
TABLE OF CONTENTS

RESERVED These details have been combined or deleted.

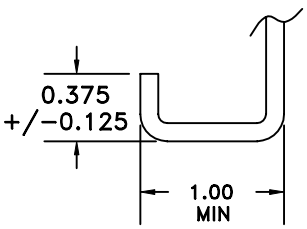
CABINET HOUSING 1 DETAIL



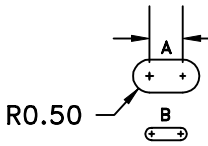
DETAIL A
CABINET HOUSINGS
VENTILATION EXHAUST DETAIL



DETAIL B
CABINET HOUSINGS
FLANGE AROUND DOOR OPENING

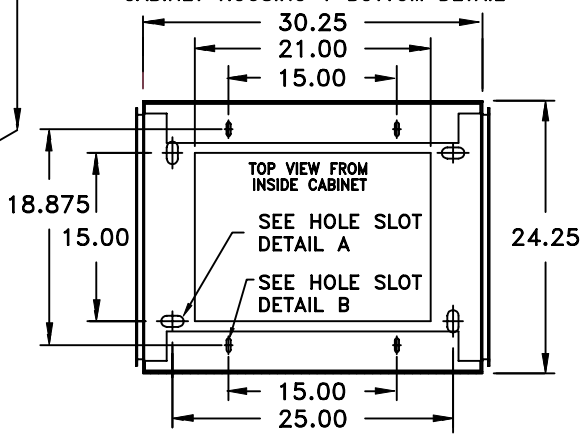


HOLE SLOT DETAIL

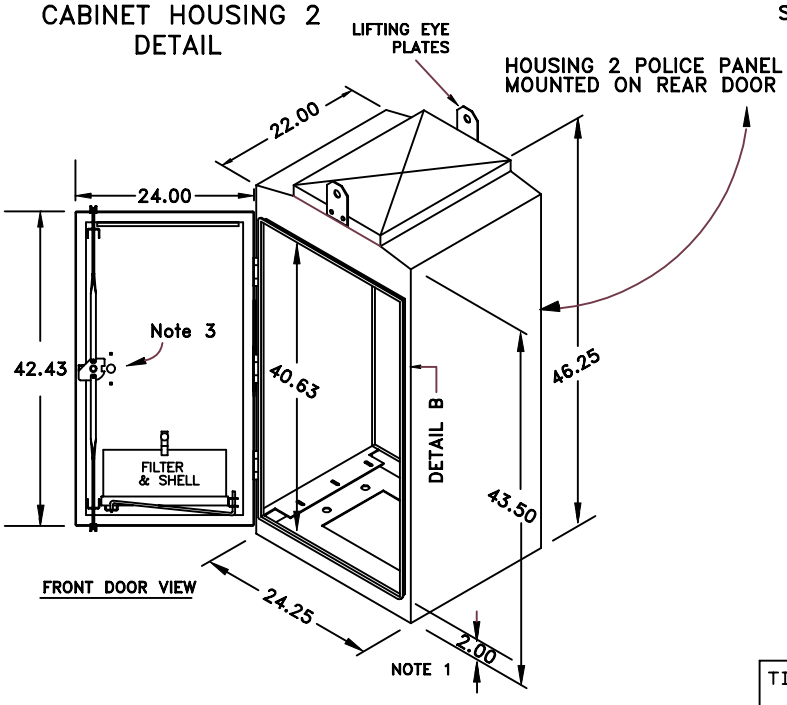


0.375X1.250 OBROUND

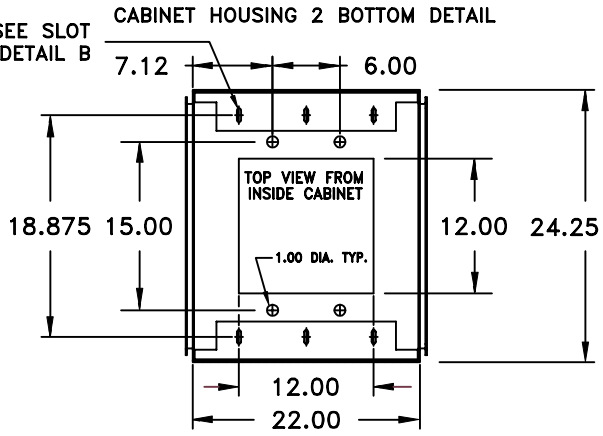
CABINET HOUSING 1 BOTTOM DETAIL



CABINET HOUSING 2 DETAIL



CABINET HOUSING 2 BOTTOM DETAIL



NOTES:

1. CABINET BASE TO DOOR OPENING.
2. ALL HOLE PATTERNS CENTERED ON CABINET BOTTOMS.
3. THE LOCKS & HANDLES SHALL BE ON THE RIGHT SIDE OF THE FRONT DOOR & THE LEFT SIDE OF THE REAR DOOR (viewed externally)

TITLE:

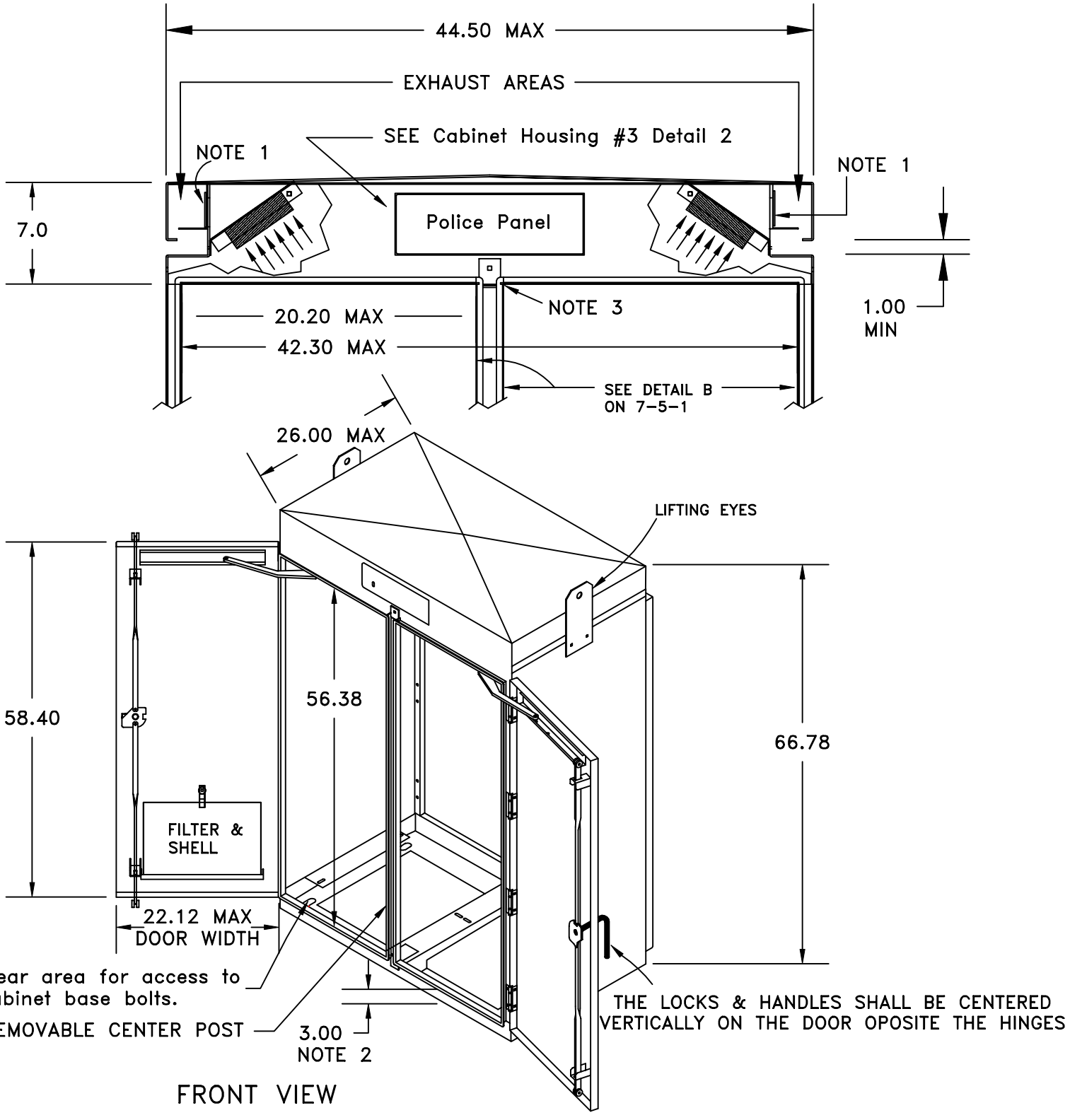
CABINET HOUSINGS 1 & 2

NO SCALE

MARCH 29, 2002

7-5-1

EXHAUST DETAIL



FRONT VIEW

NOTES:

1. PERFERATED SCREEN
2. FROM CABINET BASE TO DOOR LIP
3. AFTER CENTER POST IS INSTALLED A SEALANT SHALL BE APPLIED TO PREVENT LEAKAGE

TITLE:

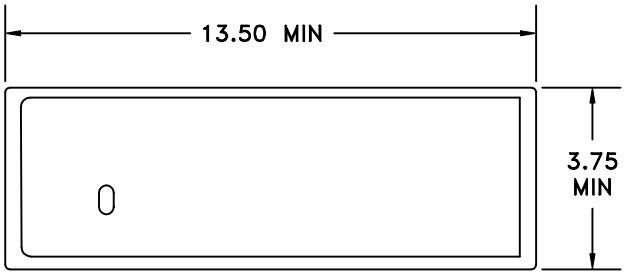
CABINET HOUSING #3
DETAIL 1

NO SCALE

MARCH 29, 2002

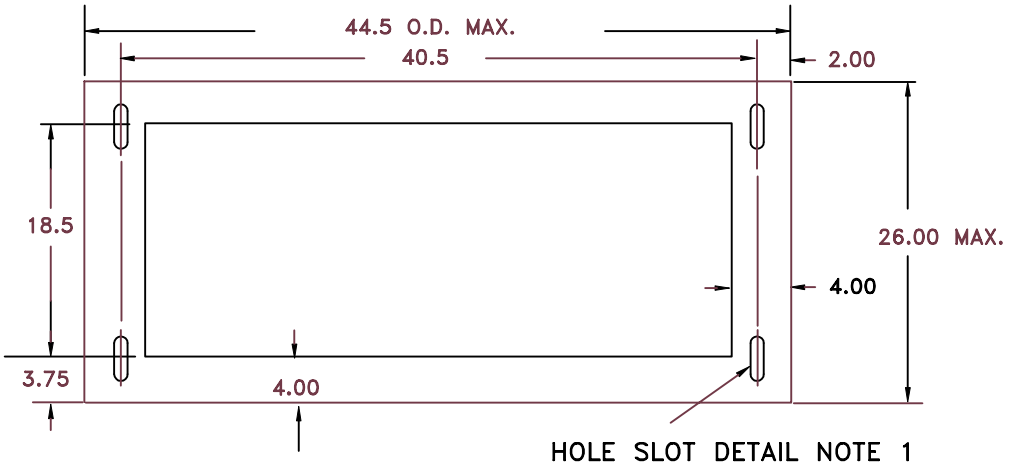
7-5-2

CABINET HOUSING #3 POLICE PANEL DETAIL

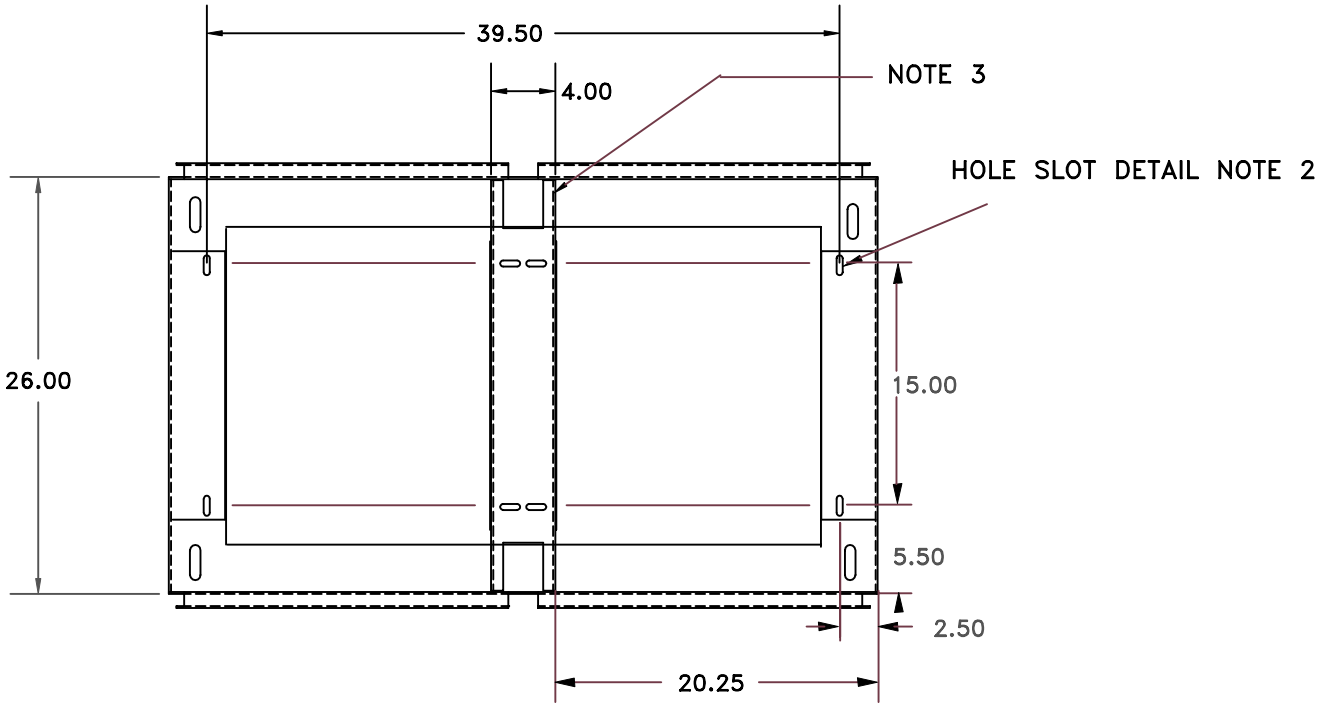


POLICE PANEL SHALL BE 3.00" MAXIMUM DEPTH

CABINET HOUSING #3 BOTTOM DETAIL



CAGE SUPPORT DETAIL (TOP VIEW)



NOTES:

1. Hole Slot Detail A see Cabinet Housings 1&2 Details
2. Hole Slot Detail B see Cabinet Housings 1&2 Details
3. Weld Cage Support to bottom assembly front and rear. See Cage Support Assembly Detail.

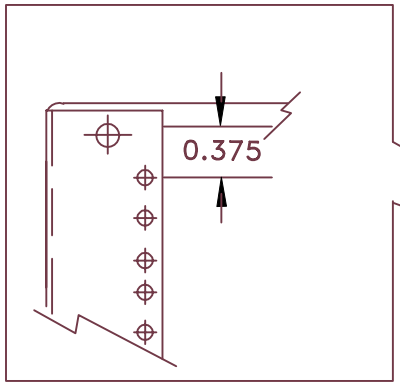
TITLE:

CABINET HOUSING #3
DETAIL 2

NO SCALE

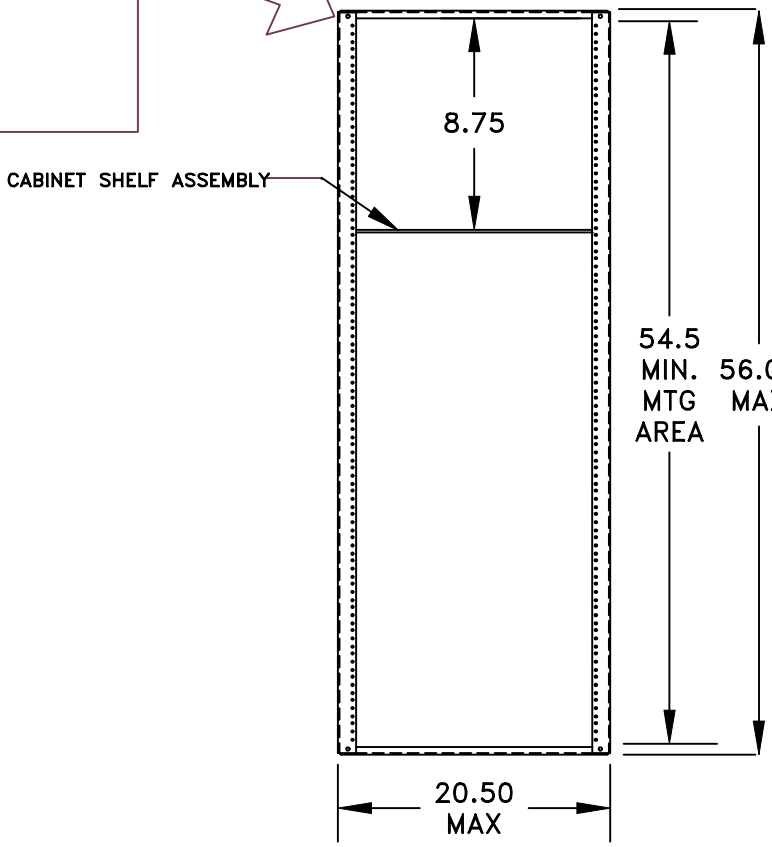
MARCH 29, 2002

7-5-3



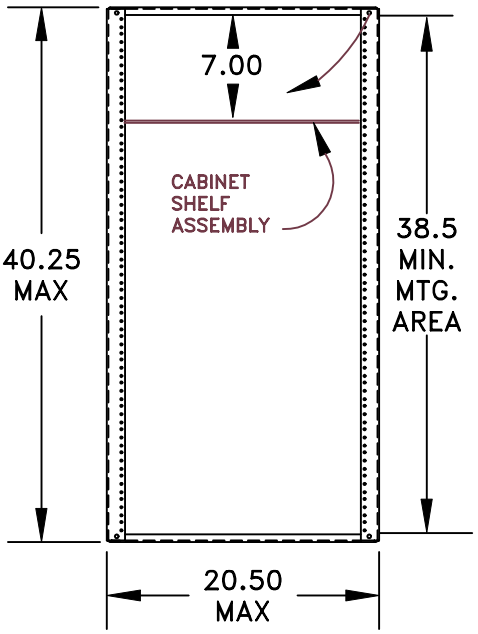
CAGE 1 DETAIL

(FRONT & REAR TYPICAL)
FRONT VIEW

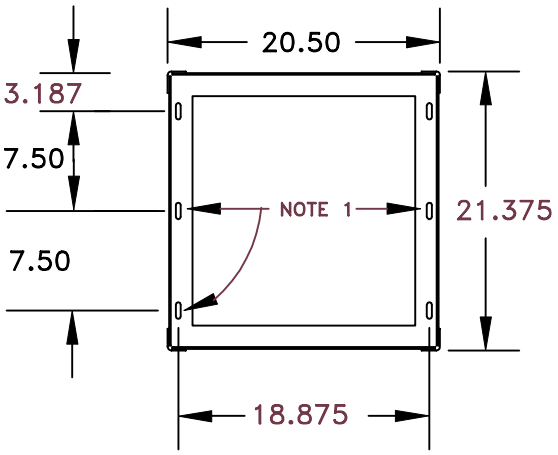


CAGE 2 DETAIL

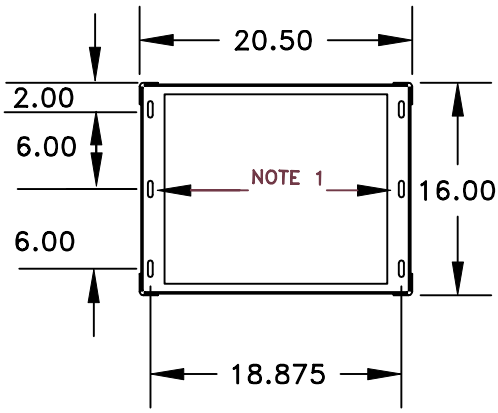
(FRONT & REAR TYPICAL)
FRONT VIEW



TOP VIEW
CAGE 1



TOP VIEW
CAGE 2

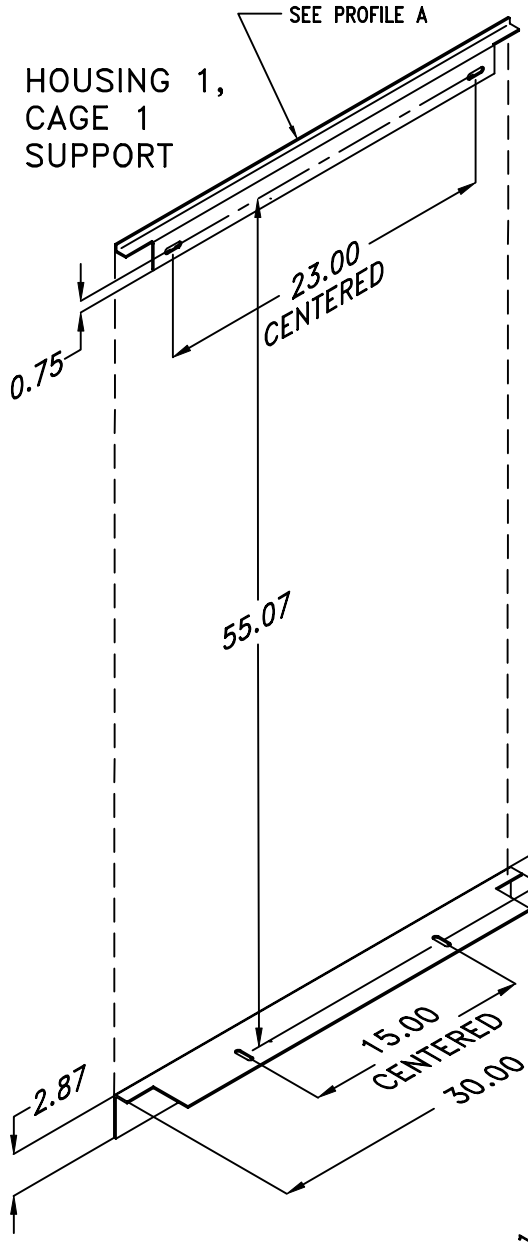


NOTES

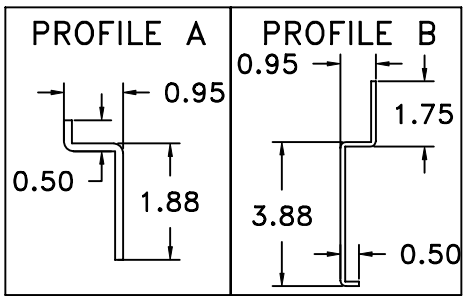
1. Hole Slot Detail B see Cabinet Housings 1&2 Details

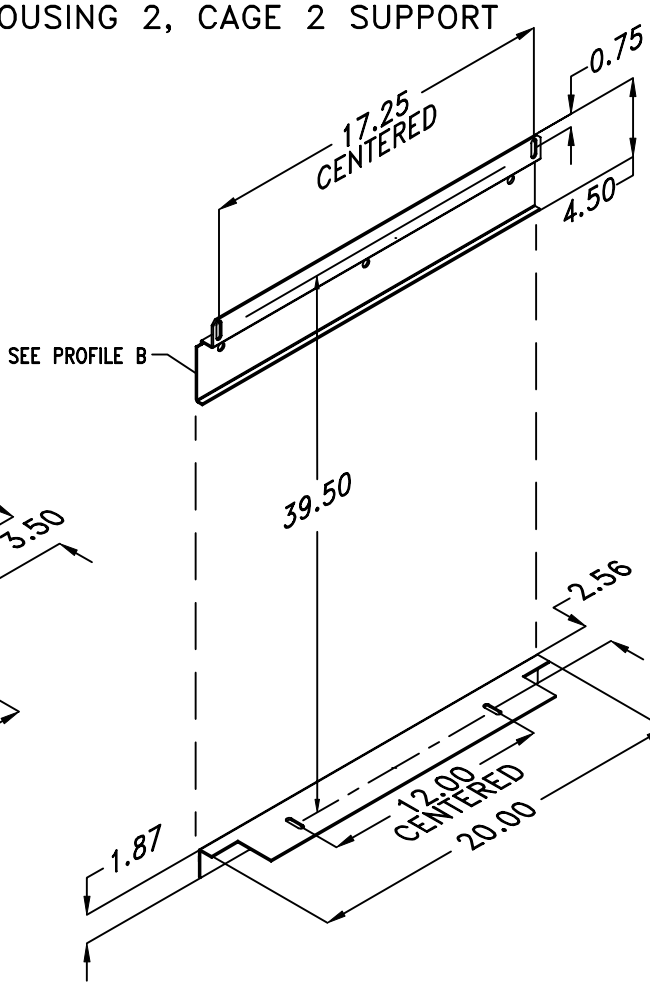
TITLE: CABINET CAGES #1 & #2	
NO SCALE	7-5-4
MARCH 29, 2002	

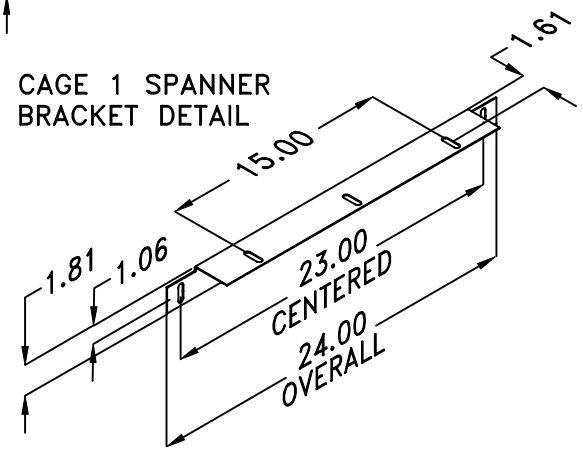
HOUSINGS 1 & 2 CAGE SUPPORT DETAILS

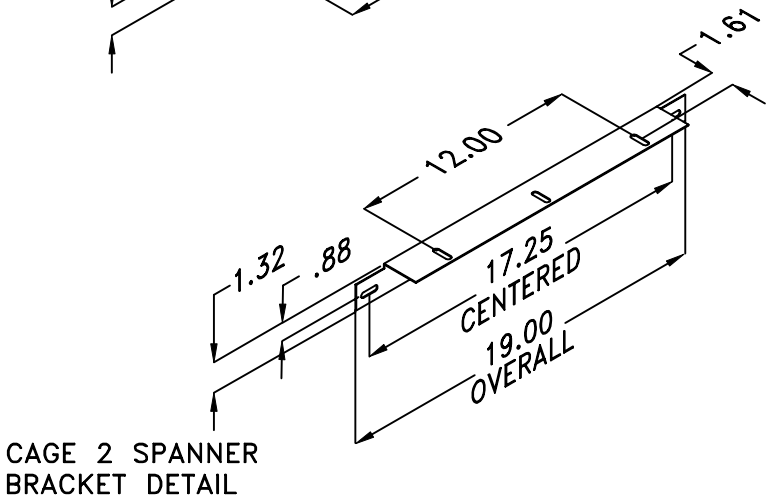


SEE HOLE SLOT DETAIL B FOR ALL SLOTS SHOWN ON THIS PAGE.







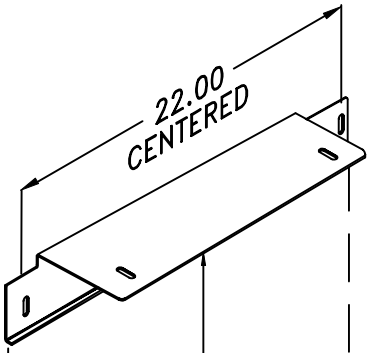


Hole Slot Detail B see Cabinet Housings 1&2 Details

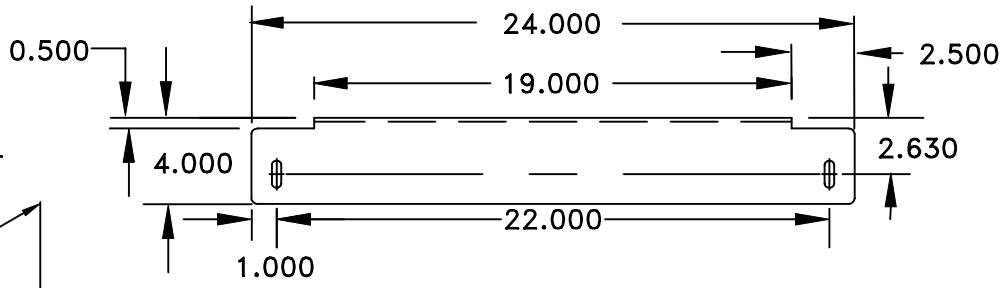
TITLE: CABINET CAGE TO HOUSING #1 & #2 SUPPORTS	
NO SCALE	7–5–5
MARCH 29, 2002	

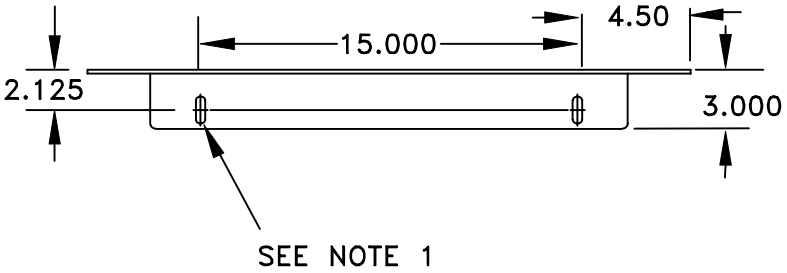
HOUSINGS 3 TO CAGE 1 SUPPORT DETAILS

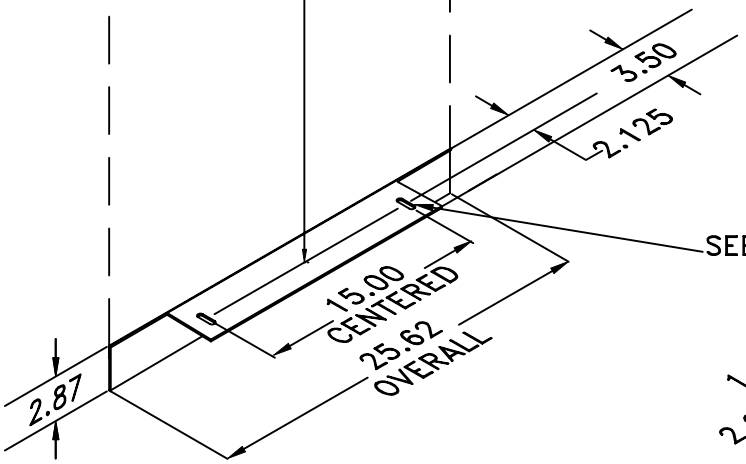
SPANNER BRACKET ATTACHED TO SIDE OF CABINET



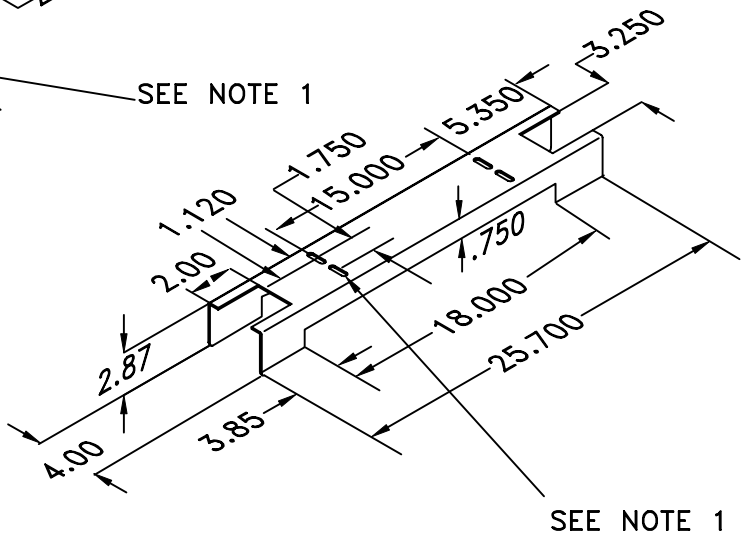
SPANNER BRACKET DETAIL







CENTER CHANNEL PART IS WELDED TO BOTTOM PLATE

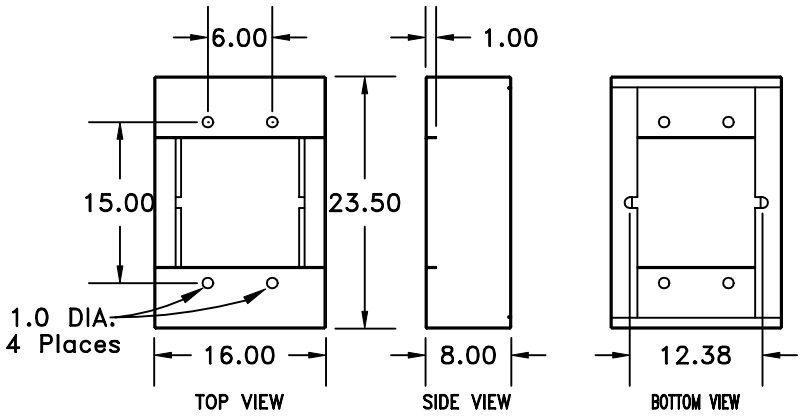


NOTES:

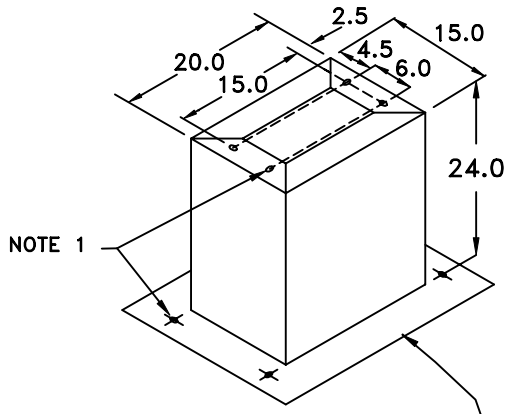
1 Hole Slot Detail B see Cabinet Housings 1&2 Details

TITLE: CABINET CAGE TO HOUSING #3 SUPPORTS	
NO SCALE	7–5–6
MARCH 29, 2002	

HOUSING 2 / M BASE ADAPTER

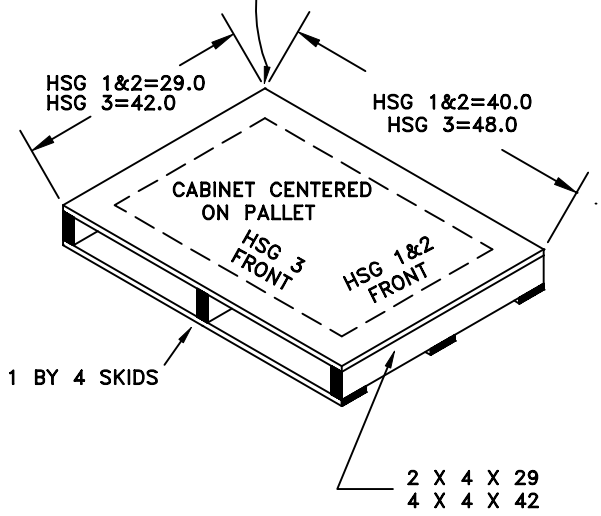


HOUSING 2 / HOUSING 1 BASE ADAPTER



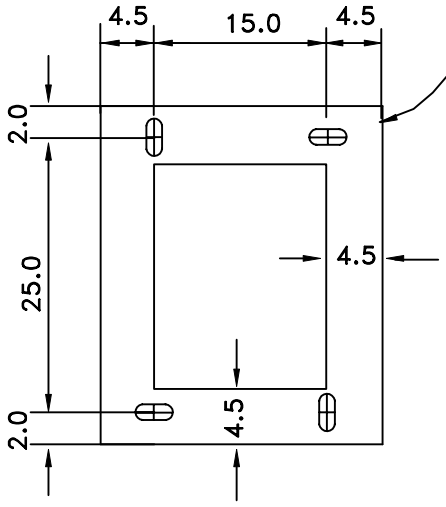
EXTERIOR PLYWOOD TOP

5/8 To 3/4 inch



CABINET SHIPPING PALLET

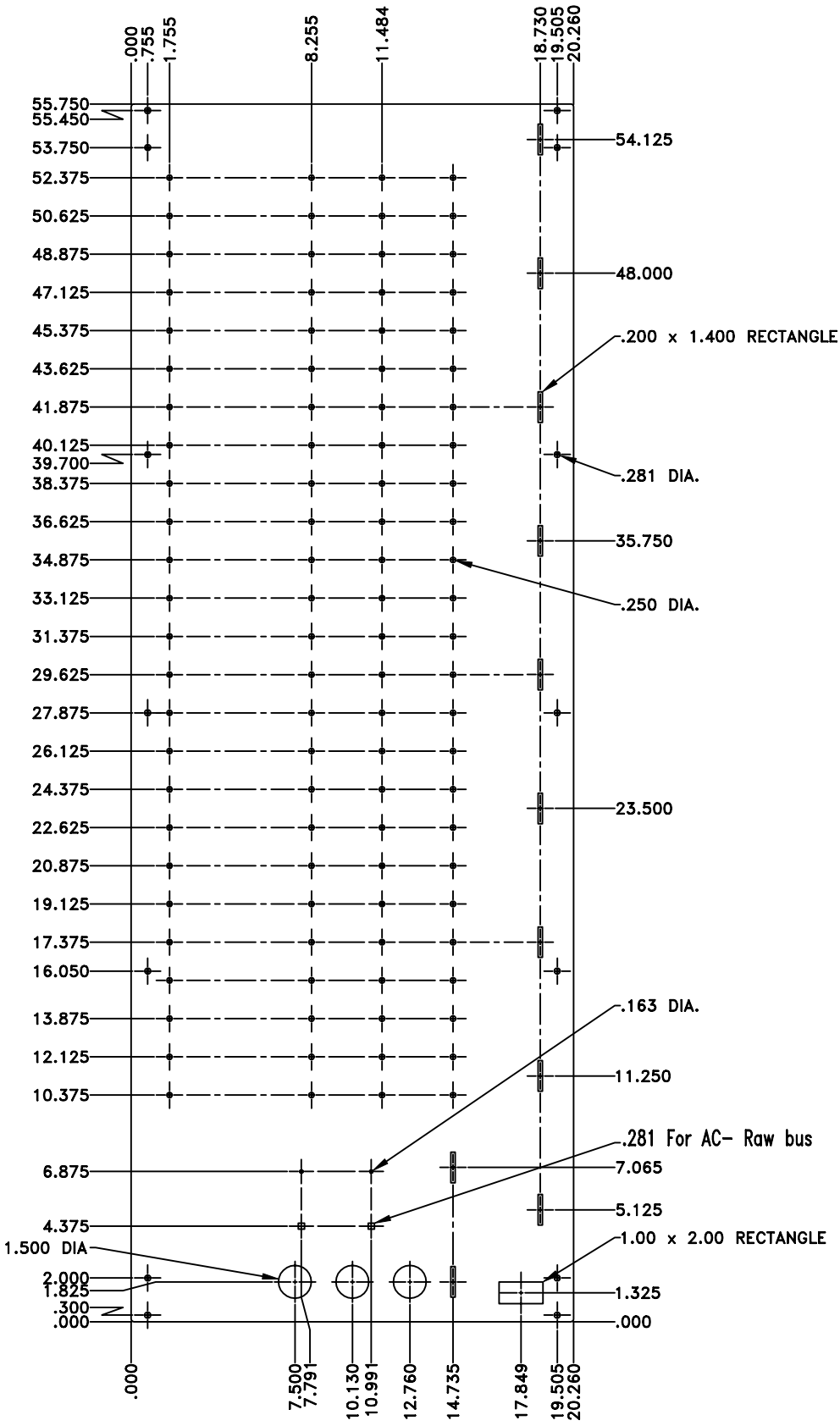
HOUSING 1 BASE VIEW



NOTES

1. Hole Slot Detail A
   See Cabinet Housings 1&2 Details

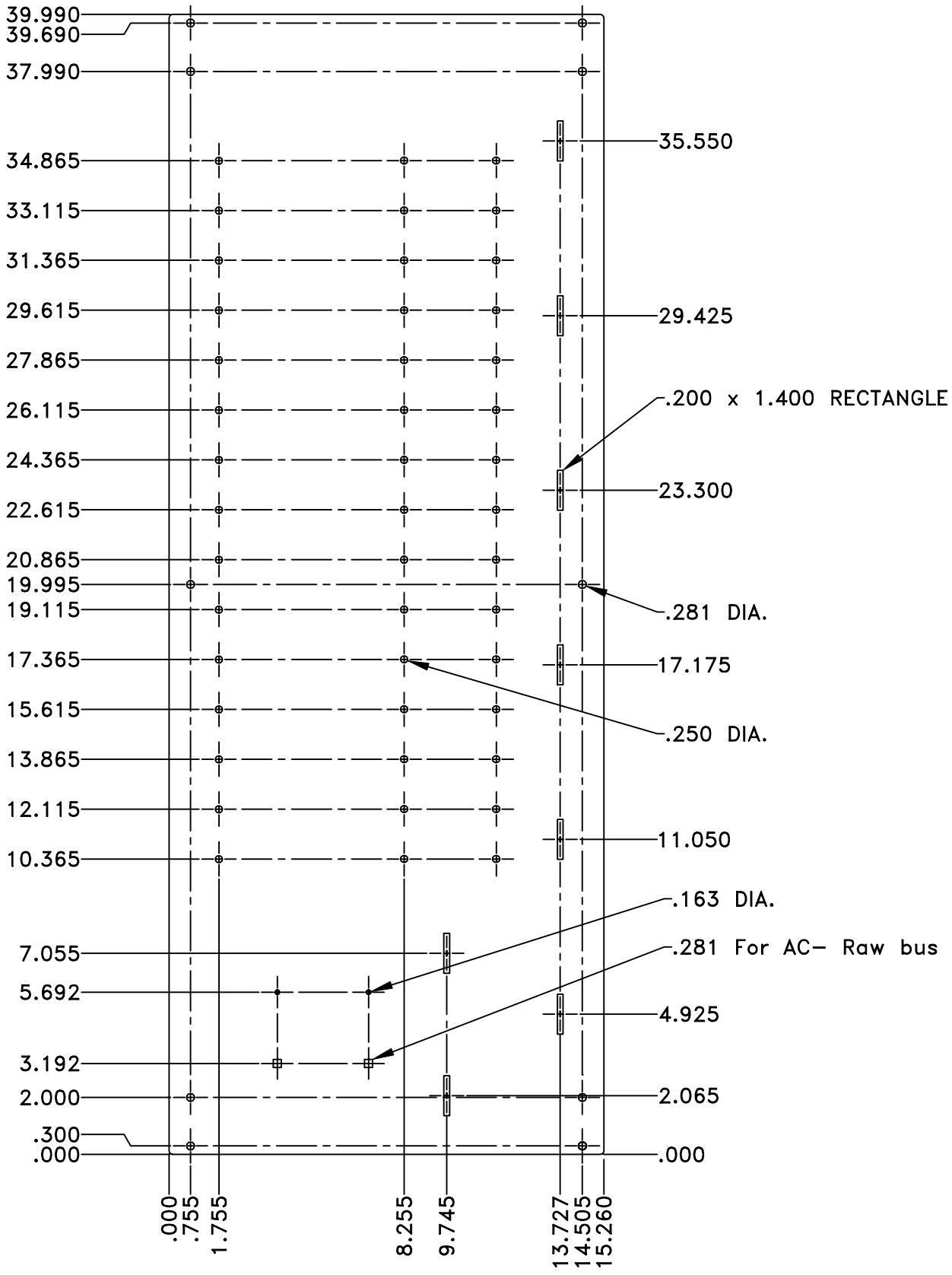
TITLE: CABINET HOUSING #2 / ADAPTERS & SHIPPING PALLET	
NO SCALE	7–5–7
MARCH 29, 2002	



NOTE:

Circular holes and rectangle shall contain grommets.

J PANEL CAGE 1	
NO SCALE	7-5-8
MARCH 29, 2002	



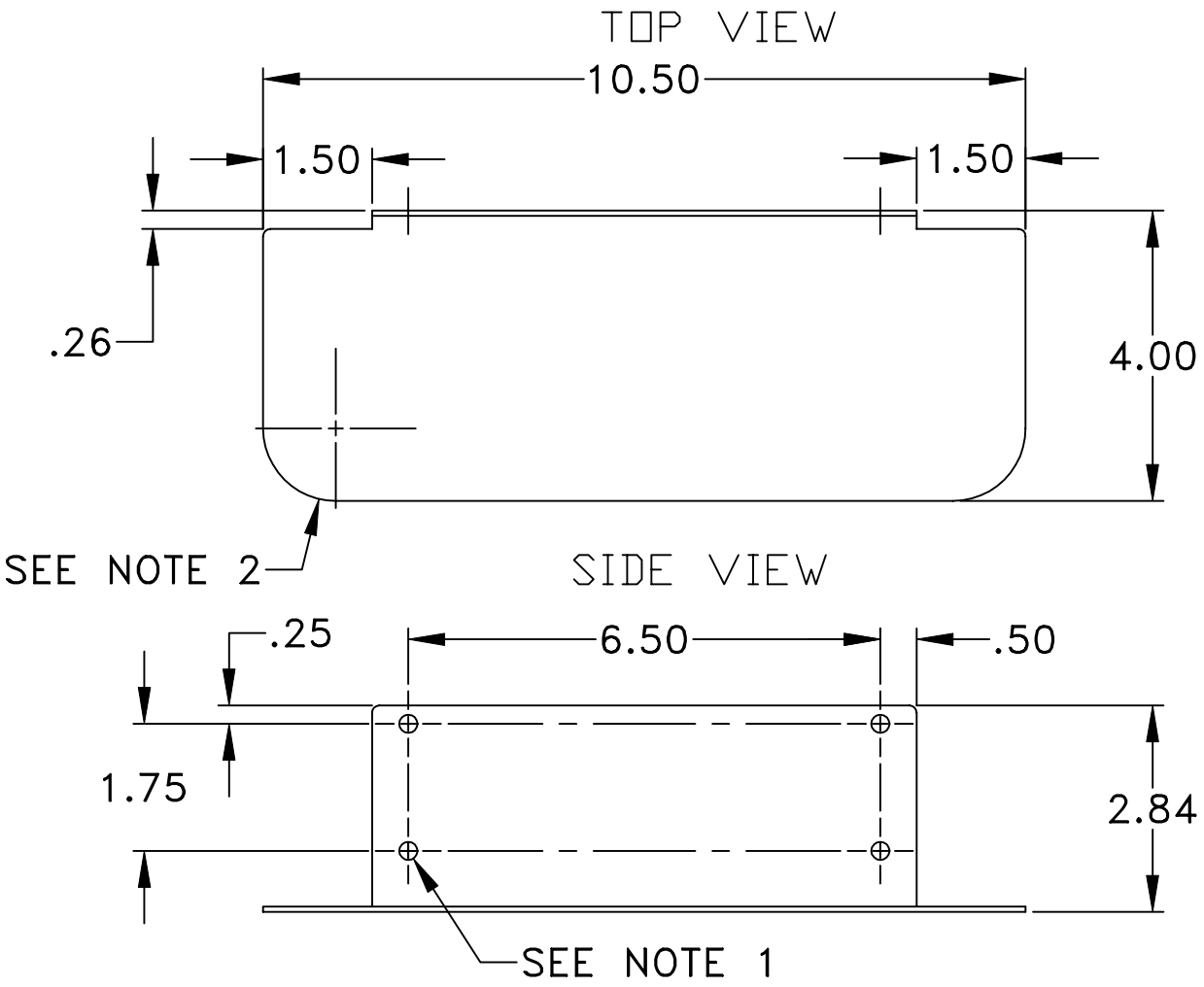
J PANEL CAGE 2

NO SCALE

MARCH 29, 2002

7-5-9

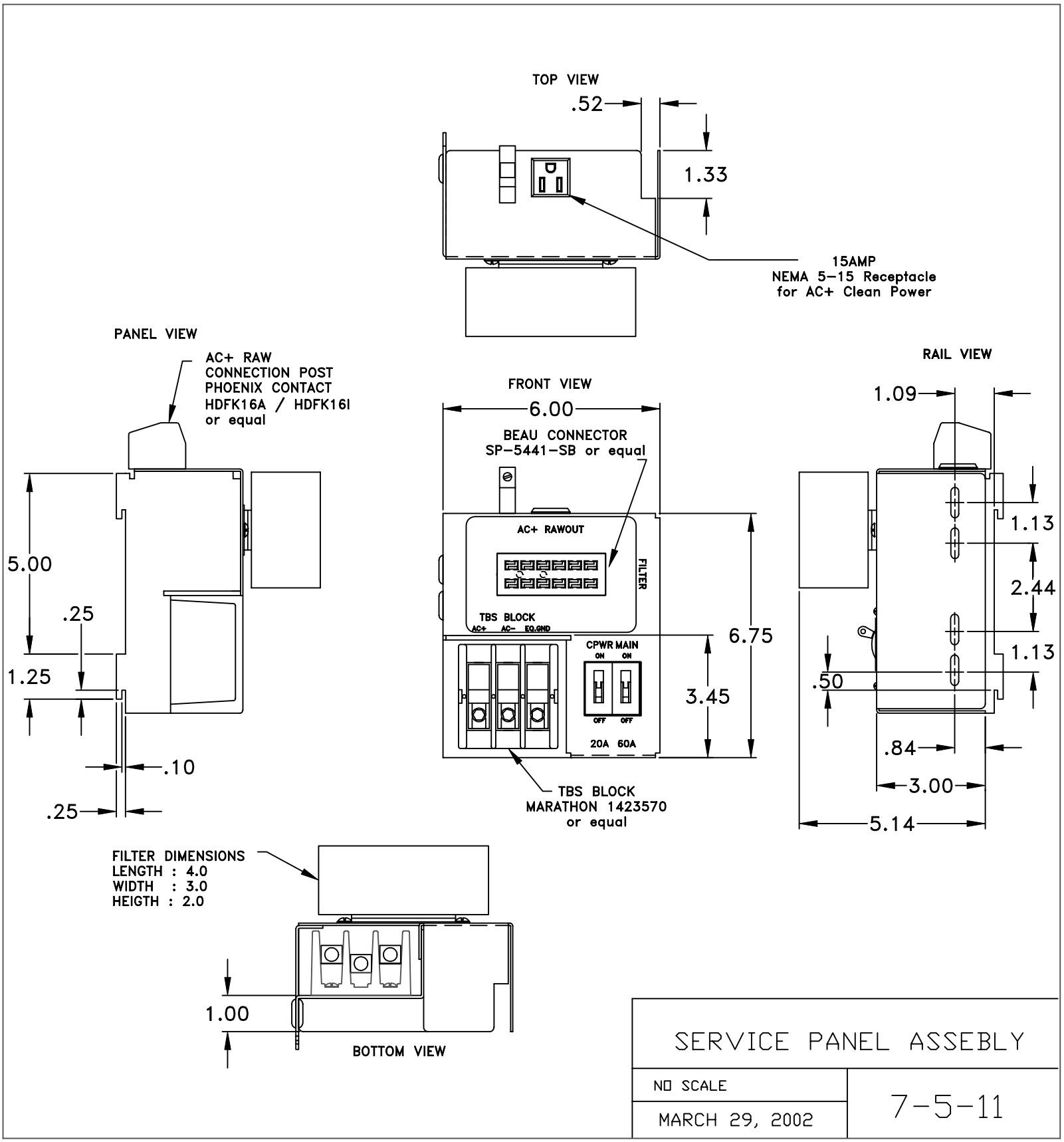
CABINET SHELF DETAIL



NOTE 1: HOLE DIA IS .250

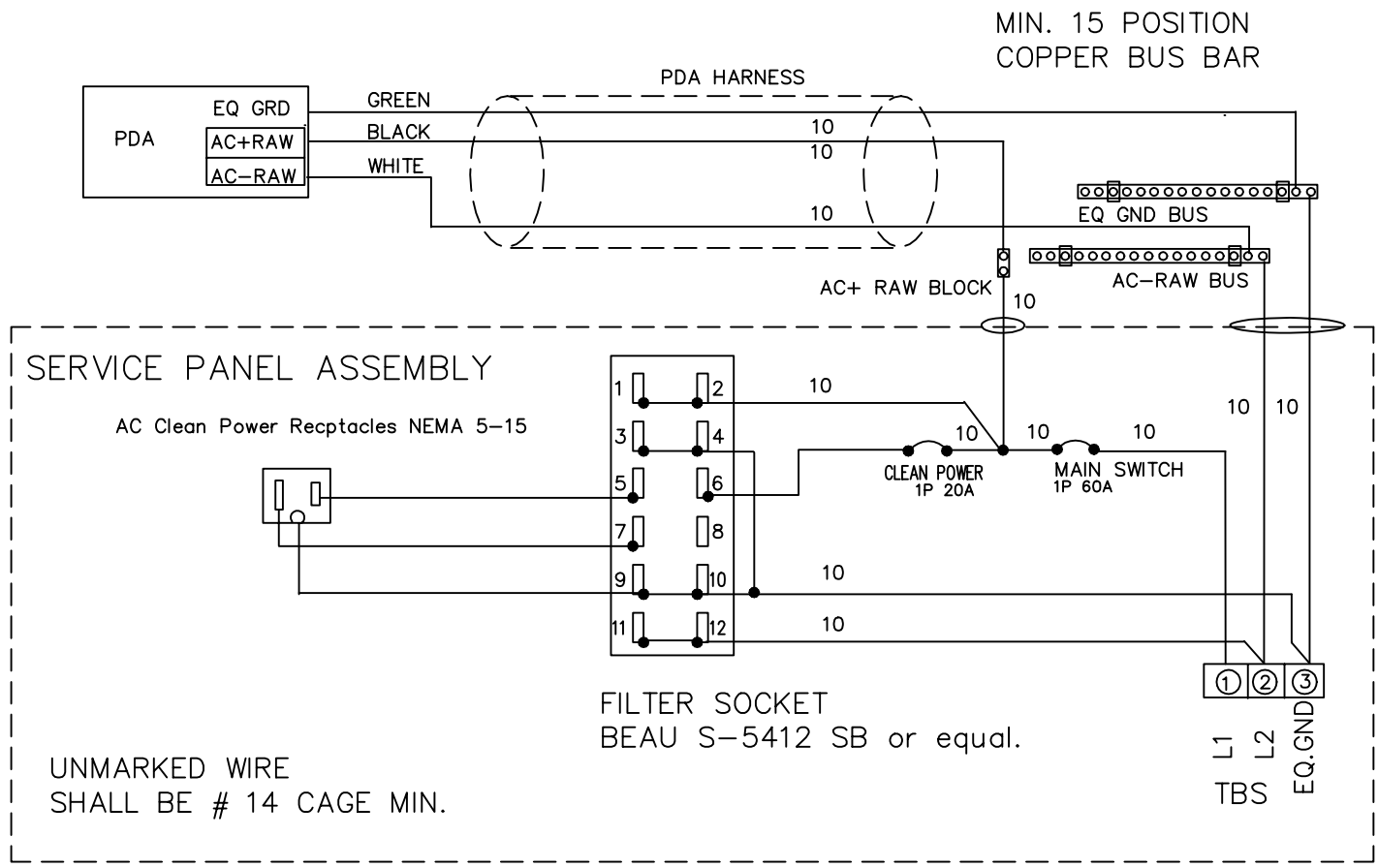
NOTE 2: RADIUS IS 1.00 R

CABINET SHELF ASSEMBLY	
NO SCALE	7-5-10
MARCH 29, 2002	



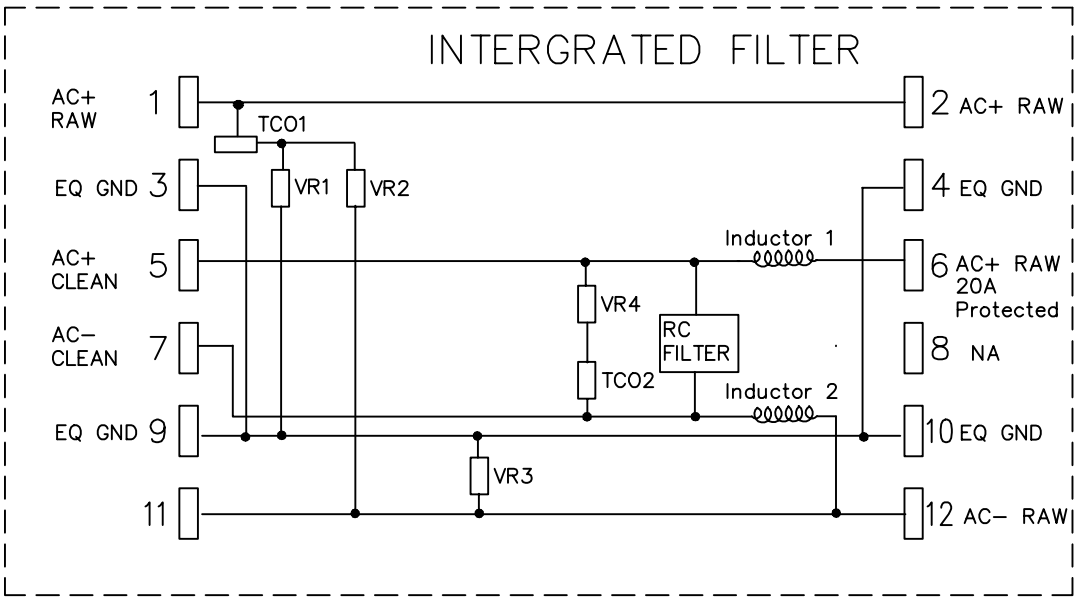
SERVICE PANEL ASSEBLY

NO SCALE	7-5-11
MARCH 29, 2002	

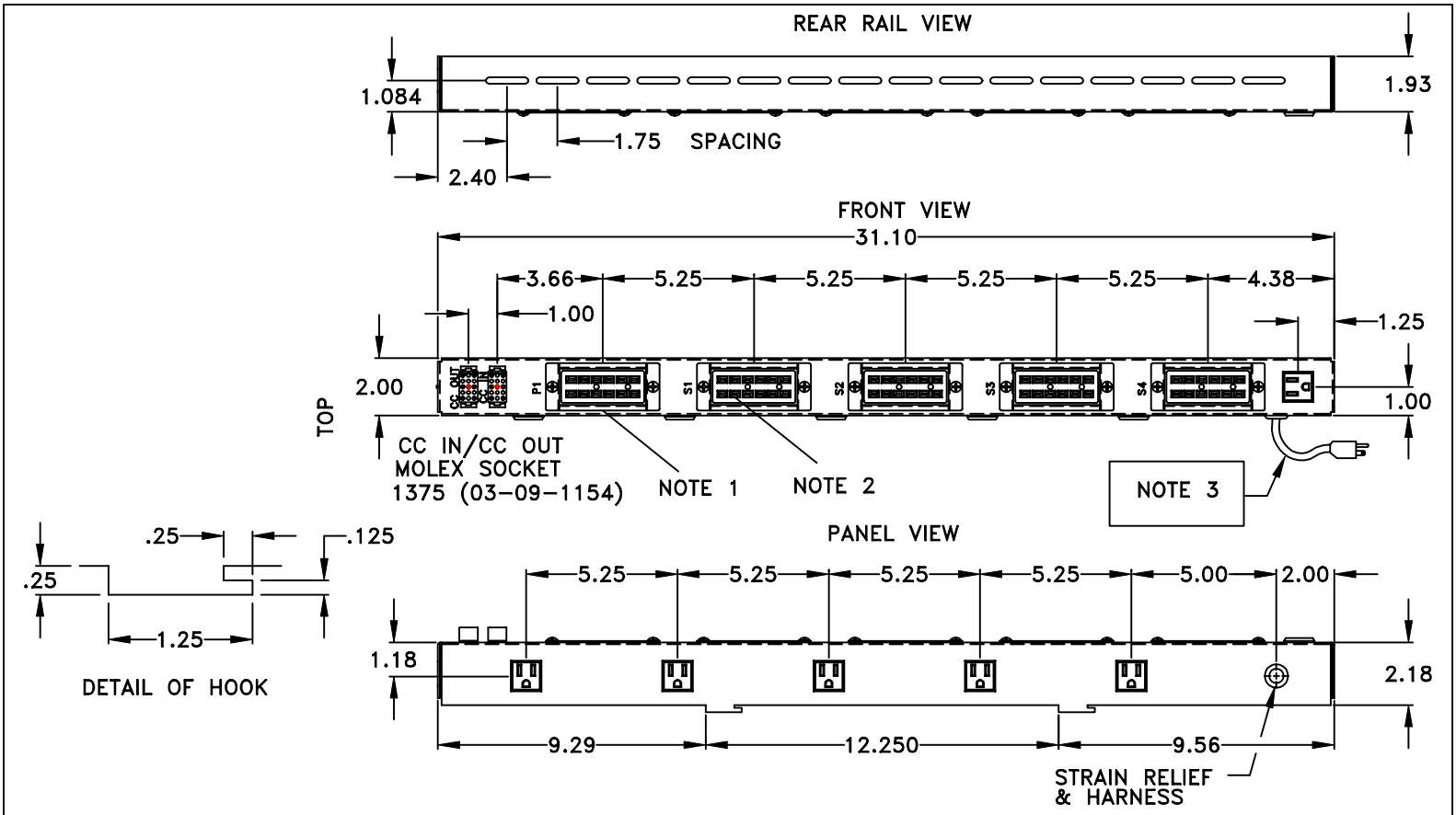


NOTES:

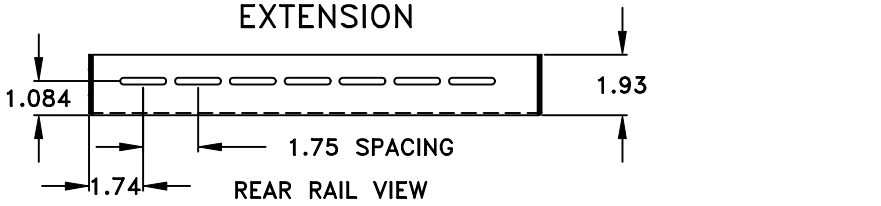
1. VR1,2 and 4 are 100 joule Movistors rated with 200V clamping
2. VR3 is 135 joule rated Movistors with 250V clamping
3. TC/TF01 and 2 Thermal Cut Off/Fuse Protection for the Movistors
4. Inductor 1 and 2 rated 30 MicroHenries at 20A
5. RC filter system 10 DB at 10 KHZ, 50 DB at 100 KHZ and 90 DB at 1 Mhz.

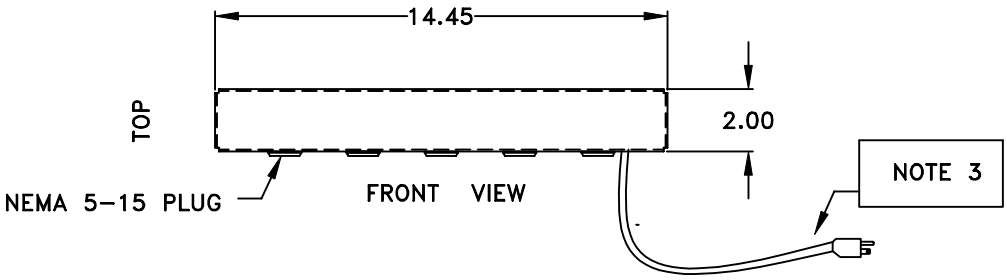


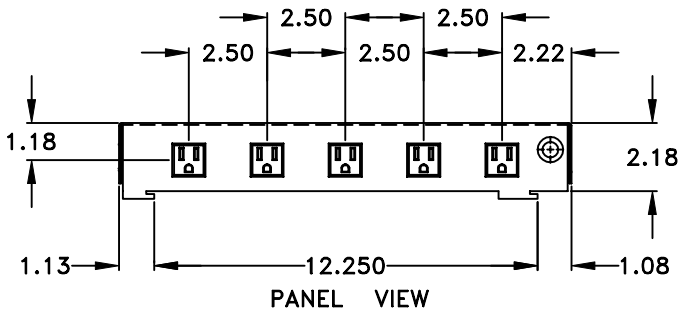
TITLE: SERVICE PANEL ASSEMBLY SCHEMATIC	
NO SCALE	7–5–12
MARCH 29, 2002	



R/C AC POWER EXTENSION





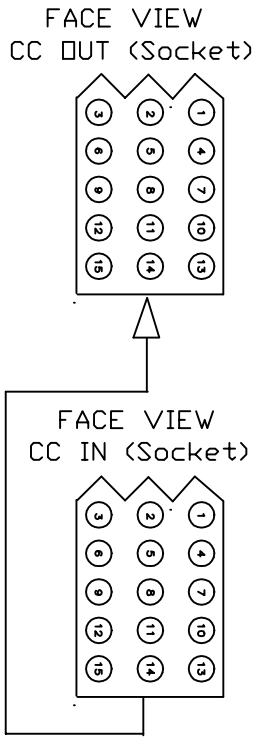


NOTES:
1. P1 – (12 CONTACT BEAU P5412-DB PLUG CONNECTOR OR EQUAL)
2. S1-S4 (12 CONTACT BEAU S5412-DB OR EQUAL)
3. HARNESS – 18 INCHES MINIMUM 3-#18 CABLE WITH 5-15 NEMA PLUG CONNECTOR

RAW/CLEAN AC POWER ASSEMBLY AND EXTENSION	
NO SCALE	7-5-15
MARCH 29, 2002	

CC CABINET CONNECTOR

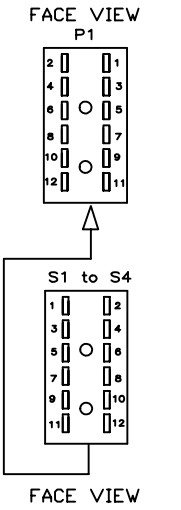
Pin #	FUNCTION	Pin #	FUNCTION
CC-1	MC COIL (From Police Panel)	CC-2	AC+ RAW
CC-3	TR COIL (From Police Panel)	CC-4	AC+ RAW
CC-5	From Front Door Switch	CC-6	From Auto / Flash Switch
CC-7	AC+ RAW Rear Door Switch	CC-8	From Rear Door Switch
CC-9	Circuit Breaker Trip Status	CC-10	AC+RAW
CC-11	AC- RAW	CC-12	STOPTIME Out
CC-13	Manual Control Enable	CC-14	INTERVAL ADV Out
CC-15	STOPTIME In		



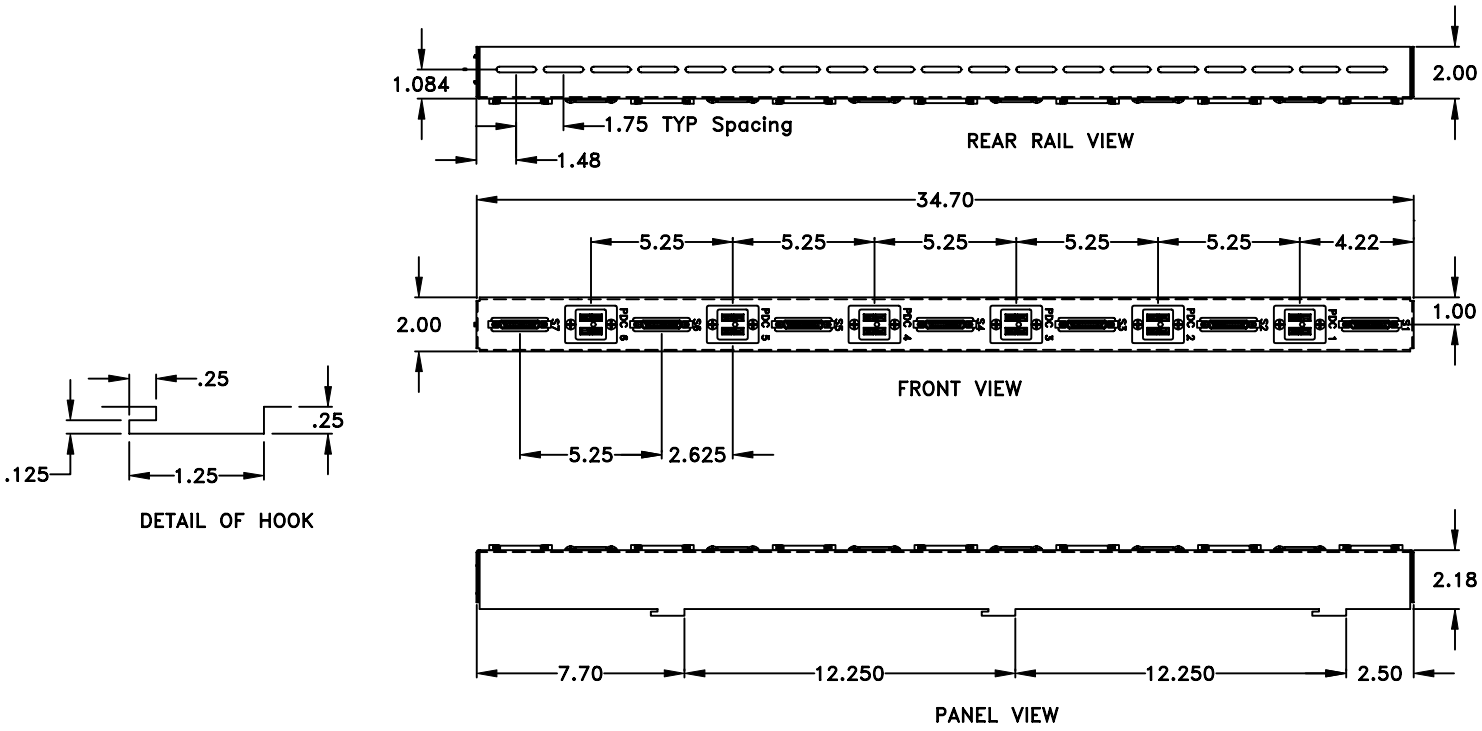
Note:
CC-3 attach to S1-9 Tr. Coil Bus
CC-10 attach to S1-10 AC+ Raw Bus
CC-11 attach to S1-11 AC- Raw Bus

ACP POWER BUS

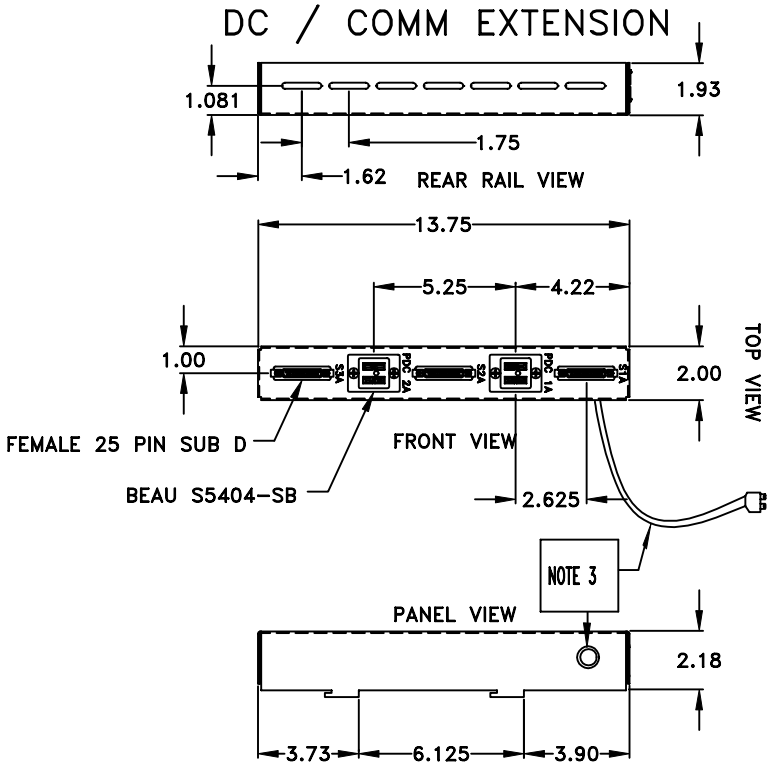
Pin	P1 INPUT AC	Pin	S1 OUTPUT ASSY 1	Pin	S2 OUTPUT ASSY 2	Pin	S3 OUTPUT ASSY 3		S4 OUTPUT ASSY 4
1	CB1 AC+	1	CB1 AC+	1	CB3 AC+	1	CB5 AC+	1	CB7 AC+
2	CB2 AC+	2	CB2 AC+	2	CB4 AC+	2	CB6 AC+	2	CB8 AC+
3	CB3 AC+	3	FU1-1	3	FU1-2	3	FU1-1	3	FU1-2
4	CB4 AC+	4	FU1-2	4	FU1-1	4	FU1-2	4	FU1-1
5	CB5 AC+	5	FU2-1	5	FU2-2	5	FU2-1	5	FU2-2
6	CB6 AC+	6	FU2-2	6	FU2-1	6	FU2-2	6	FU2-1
7	CB7 AC+	7	CB3 AC+	7		7	CB7 AC+	7	
8	CB8 AC+	8	CB4 AC+	8		8	CB8 AC+	8	
9	FU1-1	9	TR COIL DRIVE	9	TR COIL DRIVE	9	TR COIL DRIVE	9	TR COIL DRIVE
10	FU1-2	10	AC+ RAW	10	AC+ RAW	10	AC+ RAW	10	AC+ RAW
11	FU2-1	11	AC- RAW	11	AC- RAW	11	AC- RAW	11	AC- RAW
12	FU2-2	12	NA	12	NA	12	NA	12	NA



RAW/CLEAN AC POWER ASSEMBLY WIRING DIAGRAM	
NO SCALE	7-5-16
MARCH 29, 2002	



DC / COMM EXTENSION



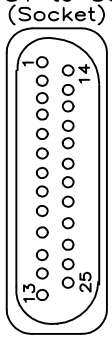
NOTES:

1. +12 and +24VDC wire shall have a minimum gauge of 14
2. SP1/SP3 shall be equivalent to CAT 5 in performance
3. Harness shall be 8 inches minimum with a BEAU P5404-LAB Plug.

DC POWER/COMMUNICATIONS ASSEMBLY & EXTENSION	
NO SCALE	7-5-17
MARCH 29, 2002	

SB1 / SB2 CONNECTOR
Referenced to ATC Controller Unit

S1 to S6
(Socket)



Pin	Function	Pin	Function
1	SB1 TXD+	14	SB1 TXD−
2	SB1 RXD+	15	SB1 RXD−
3	SB1 TXC+	16	SB1 TXC−
4	SB1 RXC+	17	SB1 RXC−
5	SB2 TXD+	18	SB2 TXD−
6	SB2 RXD+	19	SB2 RXD−
7	SB2 TXC+	20	SB2 TXC−
8	SB2 RXC+	21	SB2 RXC−
9	LINE SYNC+	22	LINE SYNC−
10	NRESET+	23	NRESET−
11	PWR DWN+	24	PWR DWN−
12	+5VDC ISO	25	EQ GND
13	ISO GND		

DCP CONNECTOR

Pin #	FUNCTION	Pin #	FUNCTION
14	+24VDC	13	+12VDC
16	DC GROUND	15	DC GROUND

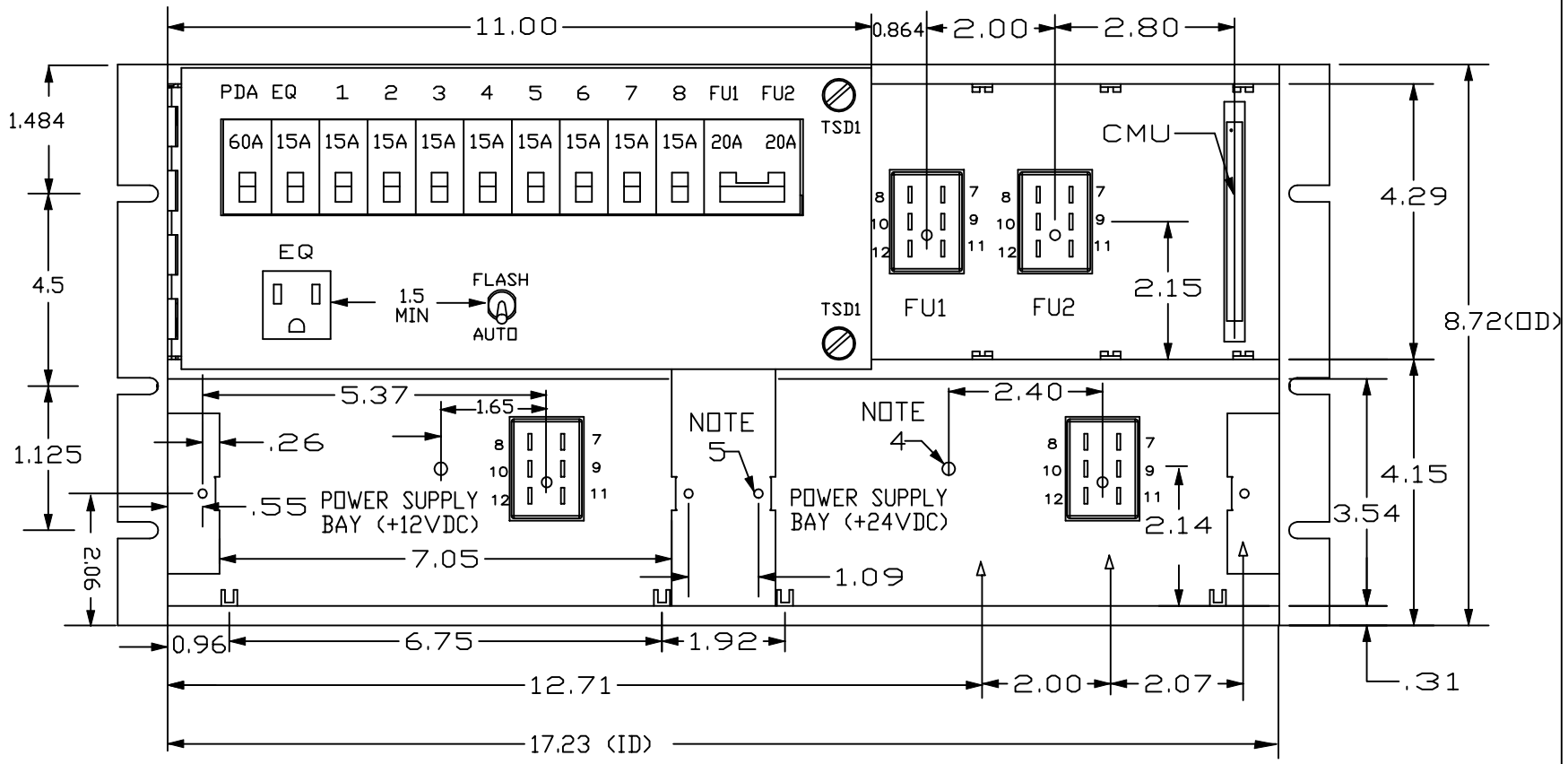
NOTES:
1. DCP Connector 1−6 is a BEAU S5404−SB or equal
2. Communications Interface shall meet CAT 5

TITLE:
DC POWER/COMMUNICATIONS ASSEMBLY WIRING DIAGRAM

NO SCALE

MARCH 29, 2002

7−5−18



NOTES:

1. FLASH UNIT (FU1&2) & POWER SUPPLY CONNECTORS SHALL BE BEAU 5406-SB OR EQUAL
2. EQ RECEPTACLE SHALL BE NEMA 5-15 SOCKET TYPE, WITH GFI PROTECTION
3. CMU CONNECTOR SHALL BE A DIN 64S OR EQUAL. SEE MODEL 212 CMU FOR PIN ASSIGNMENTS
4. CLEARANCE HOLE FOR 8-32 STUD.
5. 8-32 THREADED HOLE FOR TSD1 DEVICE.
6. ASSEMBLY DEPTH INCLUDING CONNECTORS SHALL BE 13.125 MAX.
7. → INDICATES MEASUREMENT TO CARD GUIDES FOR UPPER LEVEL

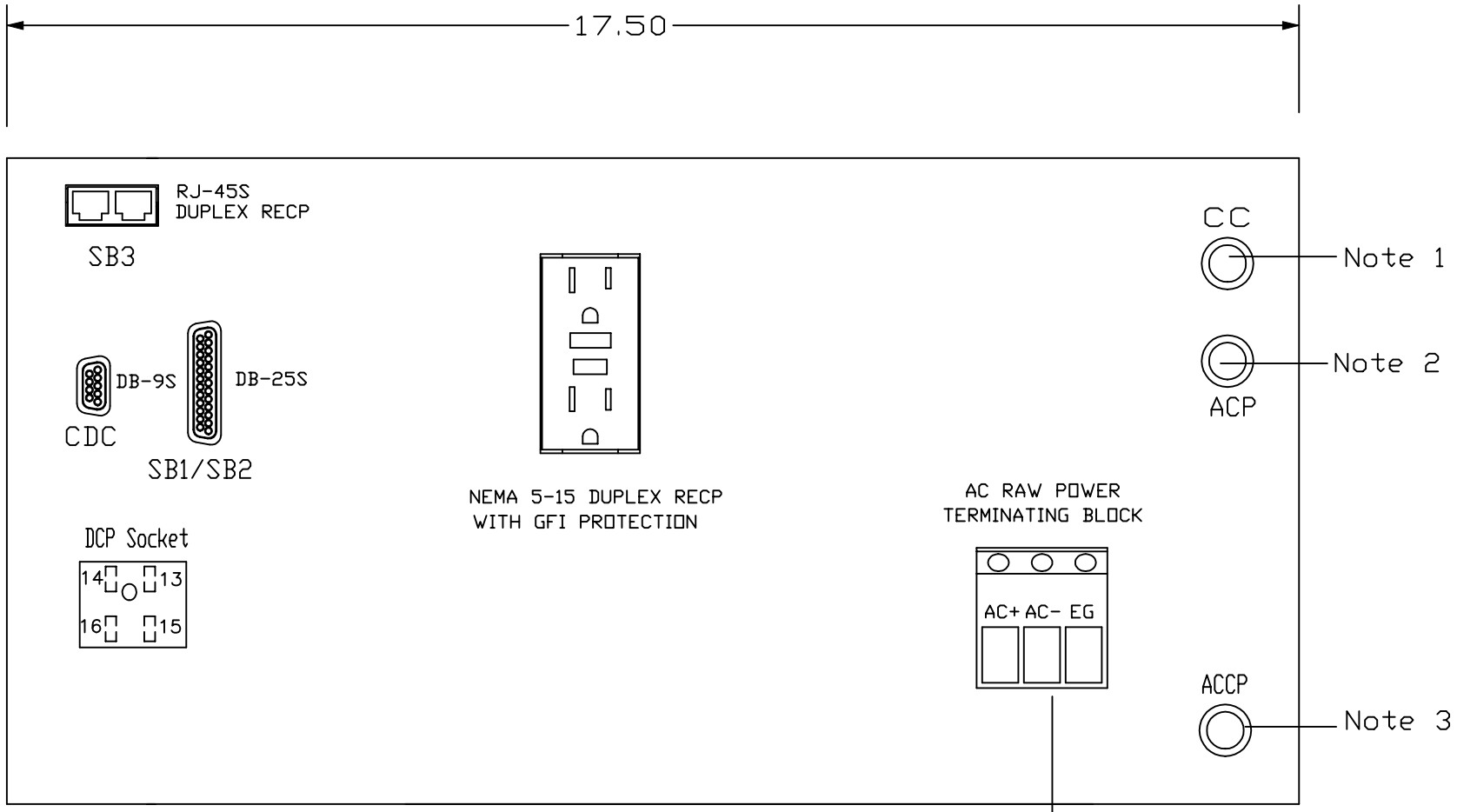
POWER SUPPLY PIN ASSIGNMENTS	FLASHER UNIT PIN ASSIGNMENTS
7 +24VDC	7 LOAD CKT #1
8 +12VDC	8 LOAD CKT #2
9 DC GND	9 EQUIP GROUND
10 EQ GND	10 AC-
11 AC-	11 AC+
12 AC+	12 NA

PINS 7-12 PARALLEL WIRED

TITLE:
PDA ITS
FRONT VIEW

NO SCALE
MARCH 29, 2002

7-5-19



NOTES:

1. CC - Harness shall be minimum 18 inches with a Molex 1375 (03-09-2159) connector or equal
2. Harness shall be minimum 18 inches with BEAU S-5412-CCE connector or equal
3. AC Clean Power Harness shall be minimum 18 inches with a NMA 5-15 Plug connector or equal
4. AC Raw Power connector shall be Phoenix Contact type HDFK 16A/HDFK16I or equal

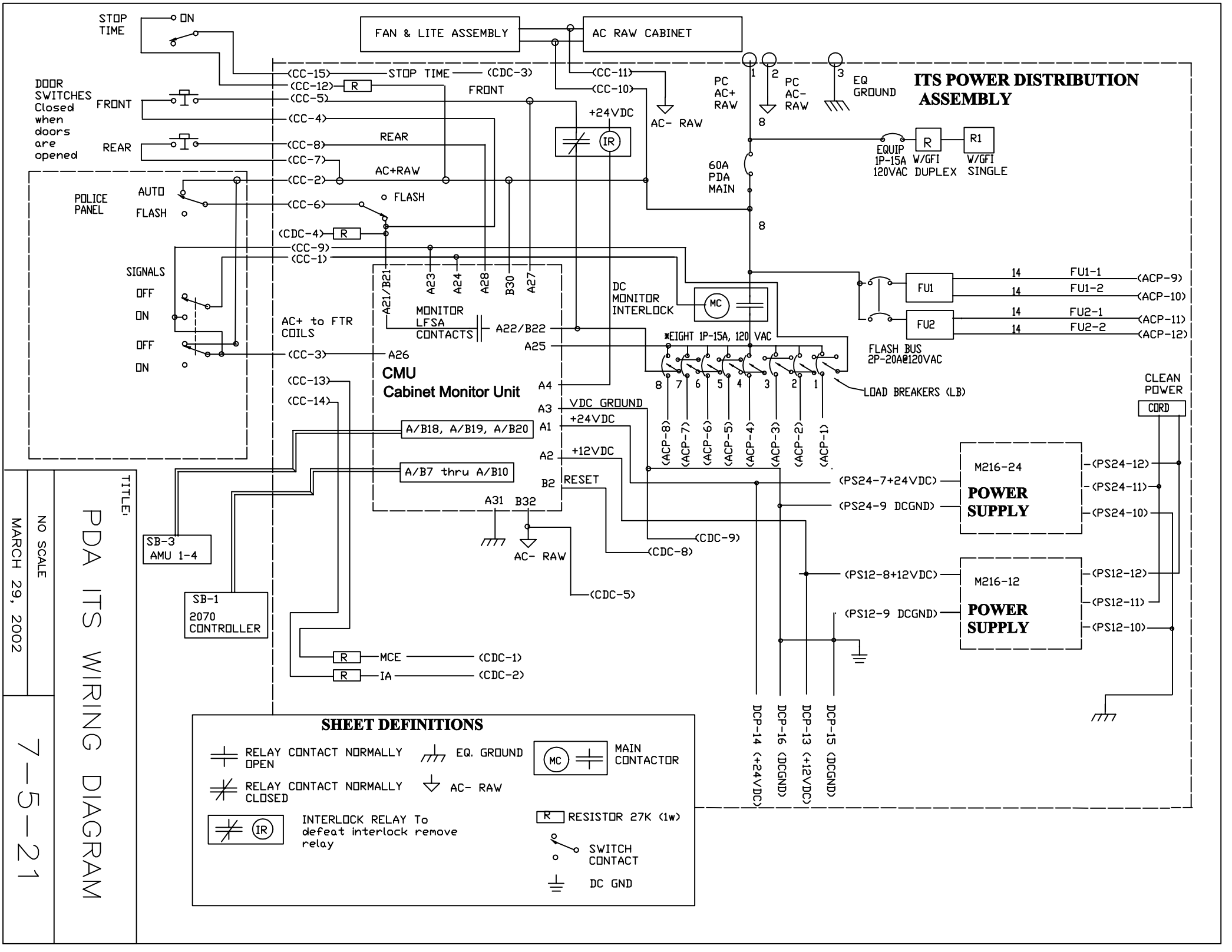
TITLE:

PDA ITS REAR VIEW

NO SCALE

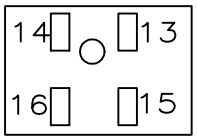
MARCH 29, 2002

7-5-20

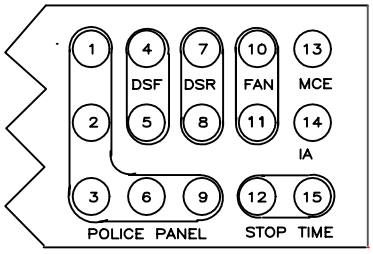

STOP TIME
ON
FAN & LITE ASSEMBLY
AC RAW CABINET
ITS POWER DISTRIBUTION ASSEMBLY
DOOR SWITCHES Closed when doors are opened
FRONT
REAR
(CC-15)
STOP TIME
(CDC-3)
(CC-12)
R
(CC-5)
(CC-4)
(CC-8)
(CC-7)
(CC-2)
AC+RAW
(CC-11)
(CC-10)
AC- RAW
+24VDC
IR
PC AC+ RAW
PC AC- RAW
EQ GROUND
60A PDA MAIN
EQUIP 1P-15A 120VAC
W/GFI DUPLEX
W/GFI SINGLE
POLICE PANEL
AUTO
FLASH
(CC-6)
(CDC-4)
(CC-9)
(CC-1)
SIGNALS
OFF
ON
(CC-3)
A26
AC+ to FTR COILS
A21/B21
A23
A24
A28
B30
A27
MONITOR LFSA CONTACTS
A22/B22
A25
DC MONITOR INTERLOCK
MC
FU1
FU2
14
FU1-1
FU1-2
FU2-1
FU2-2
(ACP-9)
(ACP-10)
(ACP-11)
(ACP-12)
*EIGHT 1P-15A, 120 VAC
FLASH BUS 2P-20A@120VAC
LOAD BREAKERS (LB)
CMU
Cabinet Monitor Unit
A4
A3
VDC GROUND
A1
+24VDC
A2
+12VDC
B2
RESET
A31
B32
AC- RAW
A/B18, A/B19, A/B20
A/B7 thru A/B10
(CC-13)
(CC-14)
(ACP-8)
(ACP-7)
(ACP-6)
(ACP-5)
(ACP-4)
(ACP-3)
(ACP-2)
(ACP-1)
CLEAN POWER
CORD
M216-24
POWER SUPPLY
(PS24-7+24VDC)
(PS24-9 DCGND)
(PS24-12)
(PS24-11)
(PS24-10)
M216-12
POWER SUPPLY
(PS12-8+12VDC)
(PS12-9 DCGND)
(PS12-12)
(PS12-11)
(PS12-10)
(CDC-9)
(CDC-8)
(CDC-5)
SB-3 AMU 1-4
SB-1 2070 CONTROLLER
MCE
IA
(CDC-1)
(CDC-2)
DCP-14 (+24VDC)
DCP-16 (DCGND)
DCP-13 (+12VDC)
DCP-15 (DCGND)
SHEET DEFINITIONS
RELAY CONTACT NORMALLY OPEN
RELAY CONTACT NORMALLY CLOSED
EQ. GROUND
AC- RAW
MAIN CONTACTOR
INTERLOCK RELAY To defeat interlock remove relay
RESISTOR 27K (1w)
SWITCH CONTACT
DC GND
TITLE:
PDA ITS WIRING DIAGRAM
NO SCALE
MARCH 29, 2002
7-5-21

PDA ITS CONNECTORS and PIN ASSIGNMENTS

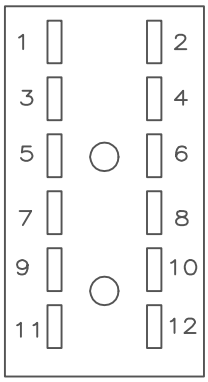
DCP (Socket)



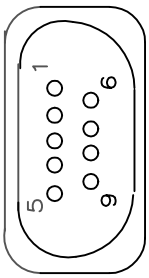
CC (Socket)



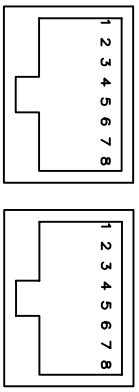
ACP (Socket)



CDC (Socket)

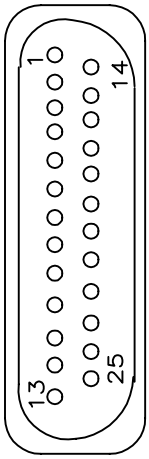


SB3 (Sockets)



SB3 SOCKETS WIRED IN PARALLEL FOR DAISY-CHAIN

SB1/SB2 (Socket)



CC (Cabinet) CONNECTOR

Pin #	FUNCTION	Pin #	FUNCTION
CC-1	MC COIL (from Police Panel)	CC-2	AC+ RAW To Police Panel
CC-3	TR Coil (from Police Panel)	CC-4	AC+ RAW To Front DS
CC-5	From Front Door Switch	CC-6	From Auto Flash Switch
CC-7	AC RAW Rear Door Switch	CC-8	From Rear Door Switch
CC-9	Circuit Breaker Trip Status	CC-10	AC+RAW
CC-11	AC- RAW	CC-12	STOP TIME Out
CC-13	MANUAL CONTROL ENABLE	CC-14	INTERVAL ADV Out
CC-15	STOP TIME in		

DCP CONNECTOR

Pin #	FUNCTION	Pin #	FUNCTION
14	+24VDC	13	+12VDC
16	DC GND	15	DC GND

PDA ITS CDC

Pin #	FUNCTION	Pin #	FUNCTION
CDC-1	MCE (Manual Control Enable)	CDC-2	IA (Interval Advance)
CDC-3	Stop Time/Monitor Relay	CDC-4	Local Flash
CDC-5	MCE,IA,Common	CDC-6	NA
CDC-7	NA	CDC-8	EXTERNAL RESET
CDC-9	DC GROUND		

ACP CONNECTOR

Pin #	FUNCTION	Pin #	FUNCTION
P-1	LB1 AC+	P-2	LB2 AC+
P-3	LB3 AC+	P-4	LB4 AC+
P-5	LB5 AC+	P-6	LB6 AC+
P-7	LB7 AC+	P-8	LB8 AC+
P-9	FU1-1	P-10	FU1-2
P-11	FU2-1	P-12	FU2-2

SB3 CONNECTOR

Pin #	PAIR COLOR	AT THE PDA	AT THE OUTPUT ASSEMBLY
1	WHITE ORANGE	SB3 TXC+	SB3 RXC+
2	ORANGE	SB3 TXC-	SB3 RXC-
3	WHITE GREEN	AC- RAW	AC- RAW
4	BLUE	SB3 TXD+	SB3 RXD+
5	WHITE BLUE	SB3 TXD-	SB3 RXD-
6	GREEN	AC- RAW	AC- RAW
7	WHITE BROWN	SB3 RXD+	SB3 TXD+
8	BROWN	SB3 RXD-	SB3 TXD-

SB1/SB2 CONNECTOR

Pin	AT THE CONTROLLER	AT THE PDA	Pin	AT THE CONTROLLER	AT THE PDA
1	SB1 TXD+	SB1 RXD+	14	SB1 TXD-	SB1 RXD-
2	SB1 RXD+	SB1 TXD+	15	SB1 RXD-	SB1 TXD-
3	SB1 TXC+	SB1 RXC+	16	SB1 TXC-	SB1 RXC-
4	SB1 RXC+	SB1 TXC+	17	SB1 RXC-	SB1 TXC-
5	SB2 TXD+	NA	18	SB2 TXD-	NA
6	SB2 RXD+	NA	19	SB2 RXD-	NA
7	SB2 TXC+	NA	20	SB2 TXC-	NA
8	SB2 RXC+	NA	21	SB2 RXC-	NA
9	LINE SYNC+	LINE SYNC+	22	LINE SYNC-	LINE SYNC-
10	NRESET+	NRESET+	23	NRESET-	NRESET-
11	PWR DWN+	PWR DWN+	24	PWR DWN-	PWR DWN-
12	+5VDC ISO	+5VDC ISO	25	EQ GND	EQ GND
13	DC GND ISO	DC GND ISO			

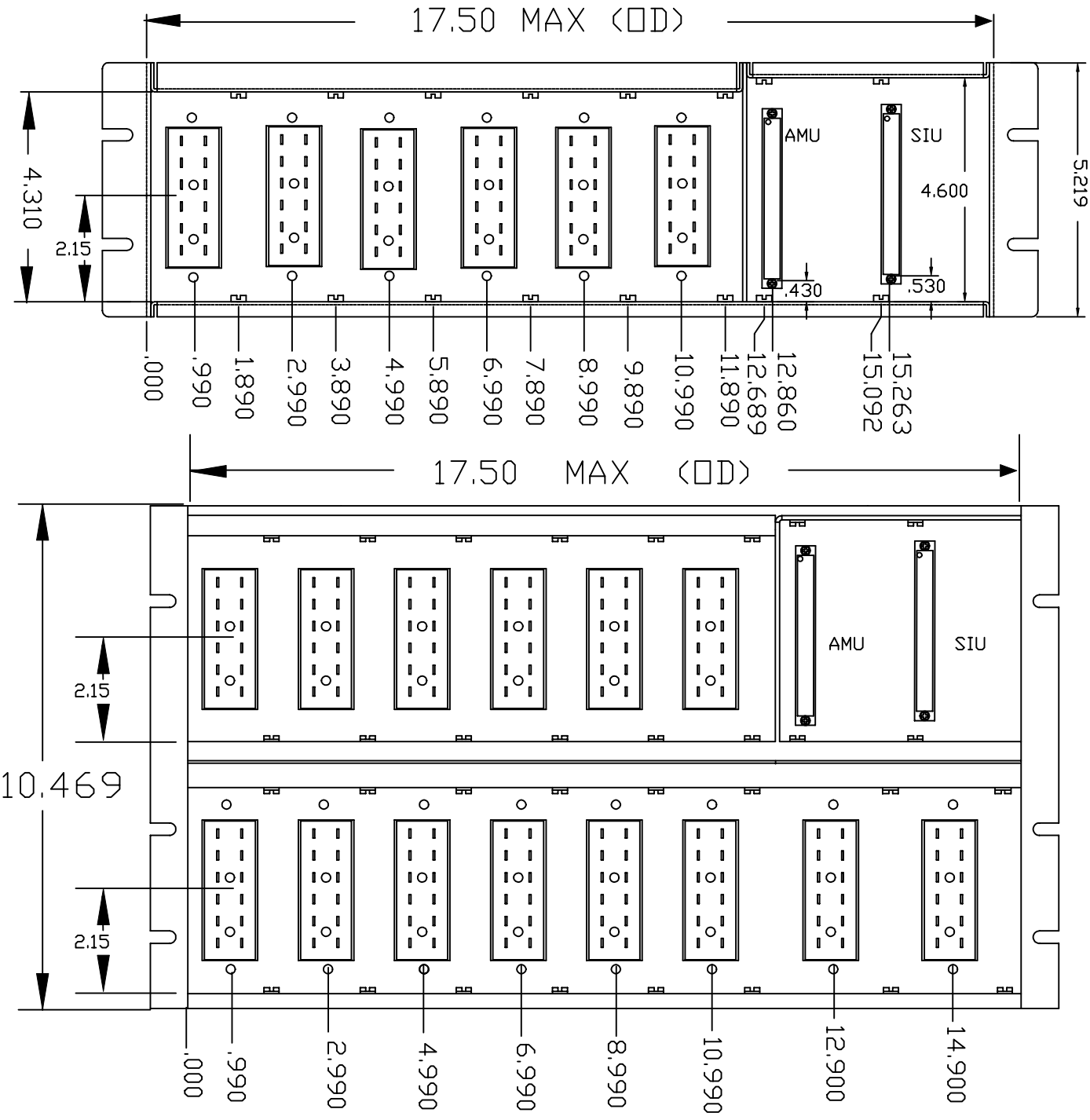
TITLE:

PDA ITS CONNECTORS

NO SCALE

MARCH 29, 2002

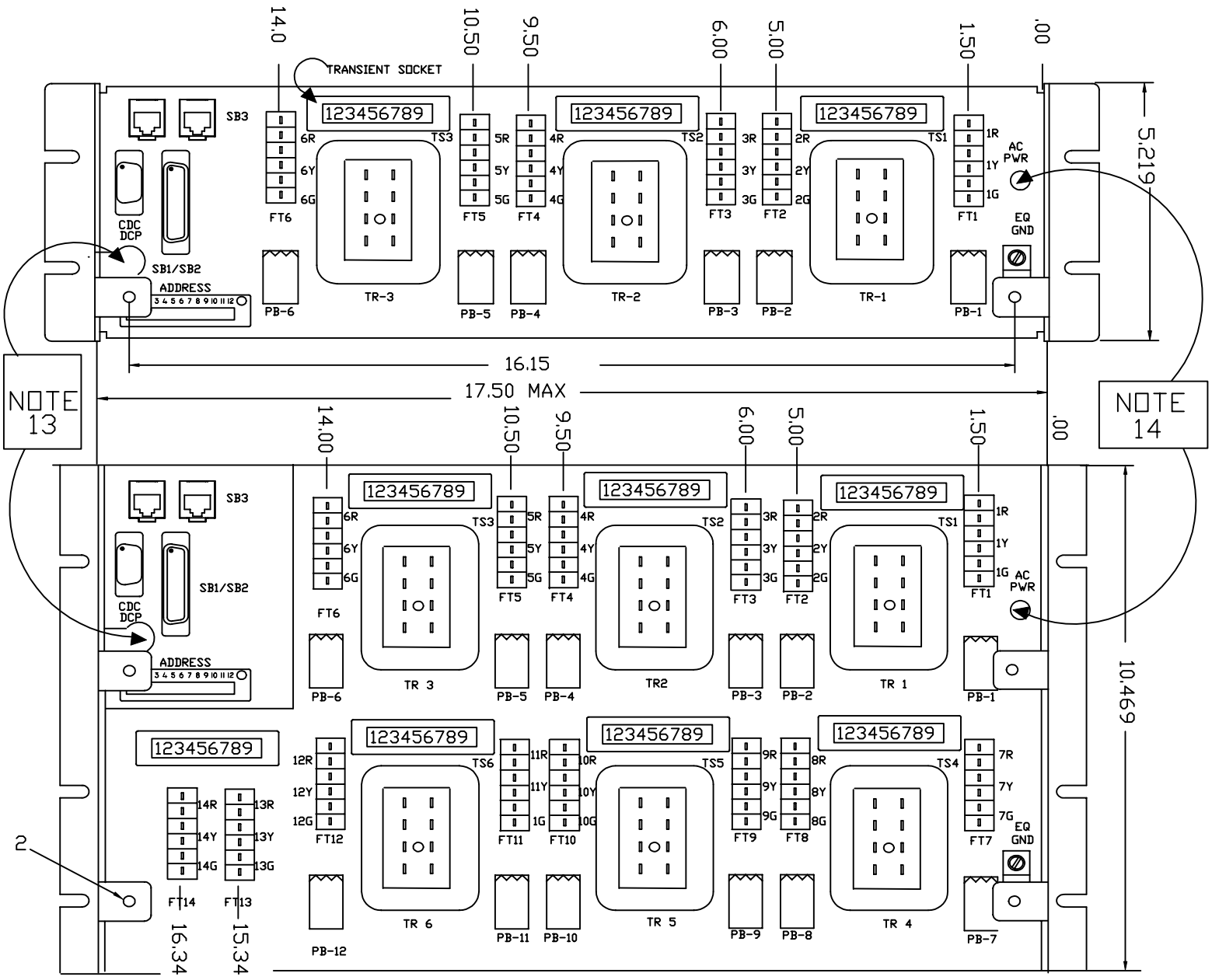
7-5-22



Notes:

1. Model 200 Switchpack Sockets shall be BEAU S-5412-S3 or equal
2. AMU and SIU Connectors shall be DIN 96 S with location same for 6 & 14 pack assemblies

6/14 PACK OUTPUT ASSEMBLY FRONT VIEW	
NO SCALE	7-5-30
MARCH 29, 2002	



NOTES:

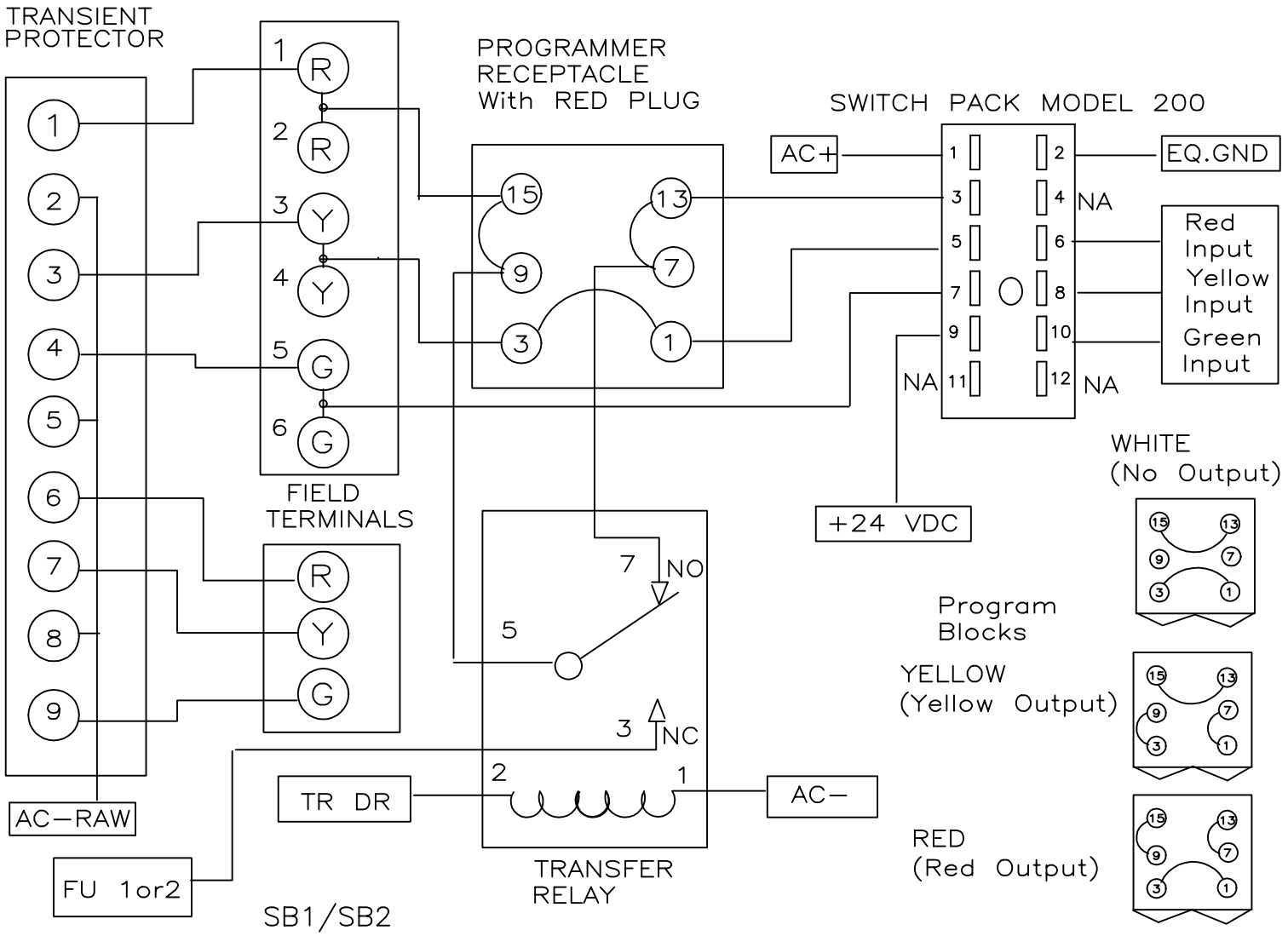
1 Maximum Assembly Depth Including Transfer Relays resident shall be 13.75
2 Wire Termination Tabs shall mate with TSD1 Thumbscrews.
3 All connectors called out shall be "or equal"
4 Transfer Relay Sockets shall be BEAU S-5408-S3
5 FIELD TERMINAL Sockets shall be Phoenix 7.62 MM (18-61-19-6)
6 FIELD TERMINAL Plugs shall be Phoenix 7.62 mm (18-04-94-6)
7 Transient Sockets shall be Phoenix 5.08 mm (07-10-24-8)
8 ADDRESS Sockets shall be 12 position Phoenix 3.81mm(18-29-43-9)
9 ADDRESS Plugs shall be 12 position Phoenix 3.81mm(18-27-22-4)
10 Program Block Sockets shall be MOLEX 1375 (03-09-1154)
11 Program Block Plugs shall be MOLEX 1375 (03-09-2159)
13 DC Power Harness shall be min. 18 inches with BEAU P9-5404-LAB with cover
14 AC Power Harness shall be min. 18" with BEAU P-5412-CCE Connector
15 EQ GND POST shall mate with a min. #10 wire.
16 CDC shall be a 9 pin D socket
17 SB1/SB2 shall be a 25Pin D socket
18 SB3 shall be a Dual 8Pin RJ45 Socket

TITLE:
6/14 OUTPUT ASSEMBLY
REAR VIEW

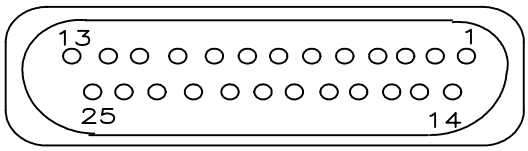
NO SCALE

MARCH 29, 2002

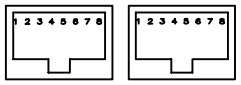
7-5-31



SB1/SB2 (Socket)



SB3 SOCKETS WIRED IN PARALLEL FOR DAISY−CHAIN



SB3 (Sockets)

SB1/SB2 CONNECTOR

Pin	AT THE CONTROLLER	AT THE OUTPUT ASSY	Pin	AT THE CONTROLLER	AT THE OUTPUT ASSY
1	SB1 TXD+	SB1 RXD+	14	SB1 TXD−	SB1 RXD−
2	SB1 RXD+	SB1 TXD+	15	SB1 RXD−	SB1 TXD−
3	SB1 TXC+	SB1 RXC+	16	SB1 TXC−	SB1 RXC−
4	SB1 RXC+	SB1 TXC+	17	SB1 RXC−	SB1 TXC−
5	SB2 TXD+	NA	18	SB2 TXD−	NA
6	SB2 RXD+	NA	19	SB2 RXD−	NA
7	SB2 TXC+	NA	20	SB2 TXC−	NA
8	SB2 RXC+	NA	21	SB2 RXC−	NA
9	LINE SYNC+	LINE SYNC+	22	LINE SYNC−	LINE SYNC−
10	NRESET+	NRESET+	23	NRESET−	NRESET−
11	PWR DWN+	PWR DWN+	24	PWR DWN−	PWR DWN−
12	+5VDC ISO	+5VDC ISO	25	EQ GND	EQ GND
13	ISO GROUND	ISO GROUND			

SB3 (CAT 5) CONNECTOR

Pin #	PAIR COLOR	AT THE PDA	AT THE OUTPUT ASSEMBLY
1	WHITE ORANGE	SP3 TXC+	SP3 RXC+
2	ORANGE	SP3 TXC−	SP3 RXC−
3	WHITE GREEN	AC− RAW	AC− RAW
4	BLUE	SP3 TXD+	SP3 RXD+
5	WHITE BLUE	SP3 TXD−	SP3 RXD−
6	GREEN	AC− RAW	AC− RAW
7	WHITE BROWN	SP3 RXD+	SP3 TXD+
8	BROWN	SP3 RXD−	SP3 TXD−

TITLE:

6/14 PACK OUTPUT ASSEMBLY WIRING DIAGRAM

NO SCALE

MARCH 29, 2002

7−5−32

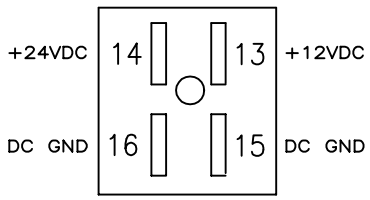
OUTPUT ASSEMBLY SIU PIN ASSIGNMENTS

PIN	SIU ROW A	SP&CDC PINS	SIU ROW B	SP&CDC PINS	SIU ROW C	TC & COMM PINS
1	+24 in	PDC−14	+24 in	PDC−14	I/O 48	NA
2	I/O 1	SP1−6	I/O 2	SP1−8	I/O 49	NA
3	I/O 3	SP1−10	I/O 4	SP2−6	I/O 50	NA
4	I/O 5	SP2−8	I/O 6	SP2−10	I/O 51	NA
5	I/O 7	SP3−6	I/O 8	SP3−8	I/O 52	NA
6	I/O 9	SP3−10	I/O 10	SP4−6	I/O 53	NA
7	I/O 11	SP4−8	I/O 12	SP4−10	I/O 54	NA
8	I/O 13	SP5−6	I/O 14	SP5−8	SB1 TxD +	Com 2 RXD+
9	I/O 15	SP5−10	I/O 16	SP6−6	SB1 TxD −	Com15 RXD−
10	I/O 17	SP6−8	I/O 18	SP6−10	SB1 RxD +	Com 1 TXD+
11	I/O 19	SP7−6	I/O 20	SP7−8	SB1 RxD −	Com14 TXD−
12	I/O 21	SP7−10	I/O 22	LS8−6	SB1 TxC +	Com 4 RXC+
13	I/O 23	SP8−8	I/O 24	SP8−10	SB1 TxC −	Com17 RXC−
14	I/O 25	SP9−6	I/O 26	SP9−8	SB1 RxC +	Com 3 TXC+
15	I/O 27	SP9−10	I/O 28	SP10−6	SB1 RxC −	Com16 TXC−
16	I/O 29	SP10−8	I/O 30	SP10−10	LINE SYNC. +	Com 9 LSync+
17	I/O 31	SP11−6	I/O 32	SP11−8	LINE SYNC. −	Com22 LSync−
18	I/O 33	SP11−10	I/O 34	SP12−6	N RESET +	Com10NRESET+
19	I/O 35	SP12−8	I/O 36	LS12−10	N RESET −	Com23NRESET−
20	I/O 37	SP13−6	I/O 38	SP13−8	ASSY ADDR	NA
21	I/O 39	SP13−10	I/O 40	SP14−6	INBUS RTS	NA
22	I/O 41	SP14−8	I/O 42	SP14−10	SB2 TxD +	NA
23	I/O 43	NA	I/O 44	NA	SB2 TxD −	NA
24	I/O 45	NA	I/O 46	NA	SB2 RxD +	NA
25	I/O 47	CDC−8	Opto 1	CDC−1	SB2 RxD −	NA
26	Opto 2	CDC−2	Opto 3	CDC−3	SB2 TxC +	NA
27	Opto 4	CDC−4	OptoComon	CDC−5	SB2 TxC −	NA
28	Address−0	ADC −1	Address−1	ADC −3	SB2 RxC +	NA
29	Address−2	ADC −5	Address−3	ADC −7	SB2 RxC −	NA
30	INBUS TxD	NA	INBUS RxD	NA	SB2 INBUS TXC	NA
31	EG	EG	AC Line Ref	NA	SB2 INBUS RxC	NA
32	DC GND	PDC−16	DC GND	PDC−16	SIU ENABLE	PDC−16

Address Connector

Pin #	FUNCT	Pin #	FUNCT
1	Addr1	2	DC GND
3	Addr2	4	DC GND
5	Addr4	6	DC GND
7	Addr8	8	DC GND
9	Addr0	10	Common
11	Addr1	12	Common

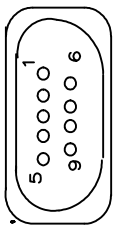
DCP(Plug)
PLUG (Face View)



CDC Connector

Pin	FUNCTION	Pin	FUNCTION
1	OPTO 1	6	NA*
2	OPTO 2	7	NA*
3	OPTO 3	8	A25 I/O−47
4	OPTO 4	9	B24 VDC Ground
5	OPTO COMON		

CDC
(Socket Face View)



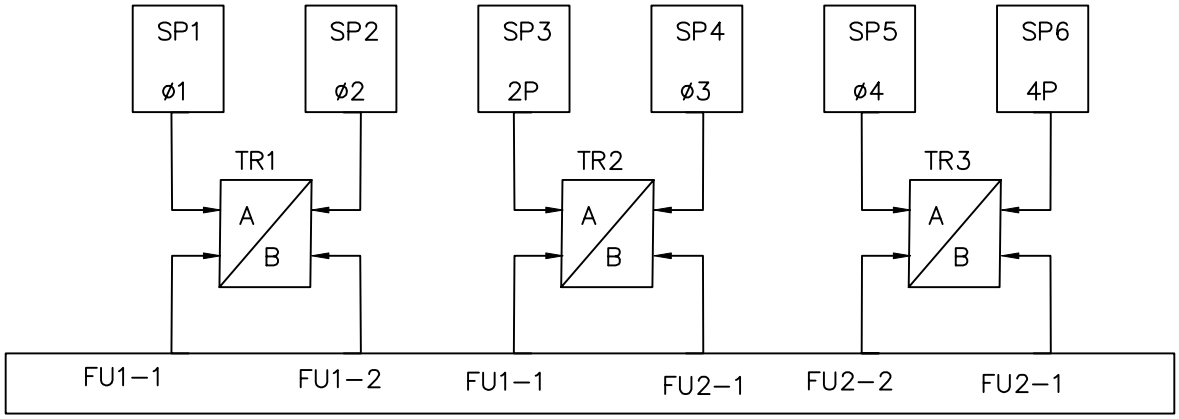
TITLE:

6/14 PACK OUTPUT ASSEMBLY CONNECTORS

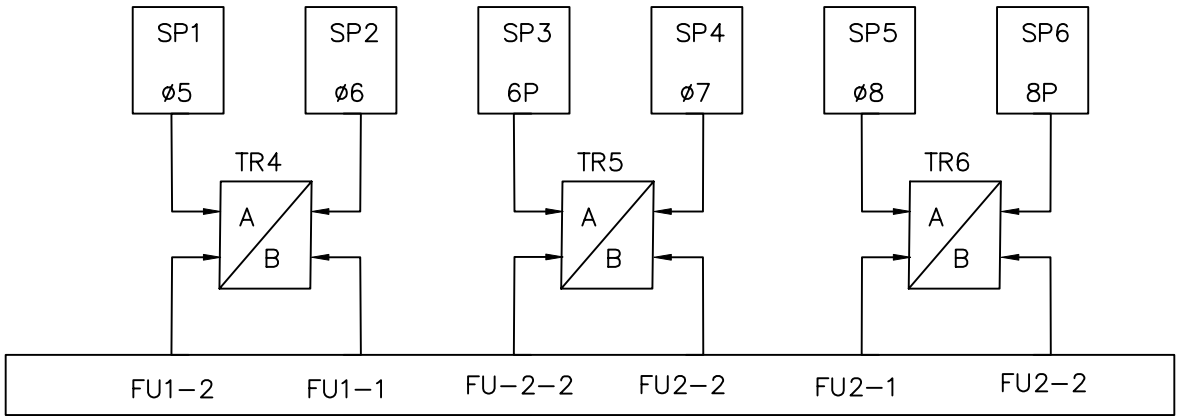
NO SCALE

MARCH 29, 2002

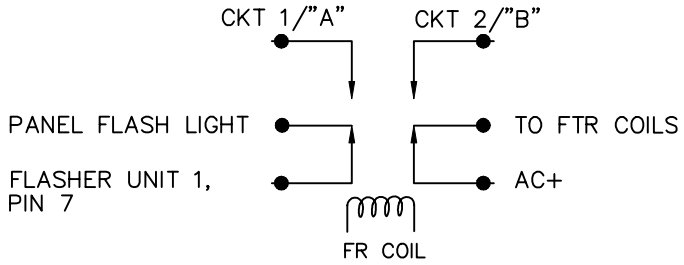
7−5−33



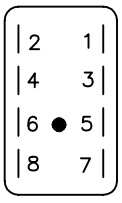
FLASHER TO OUTPUT ASSIGNMENT



FLASHER TO OUTPUT ASSIGNMENT



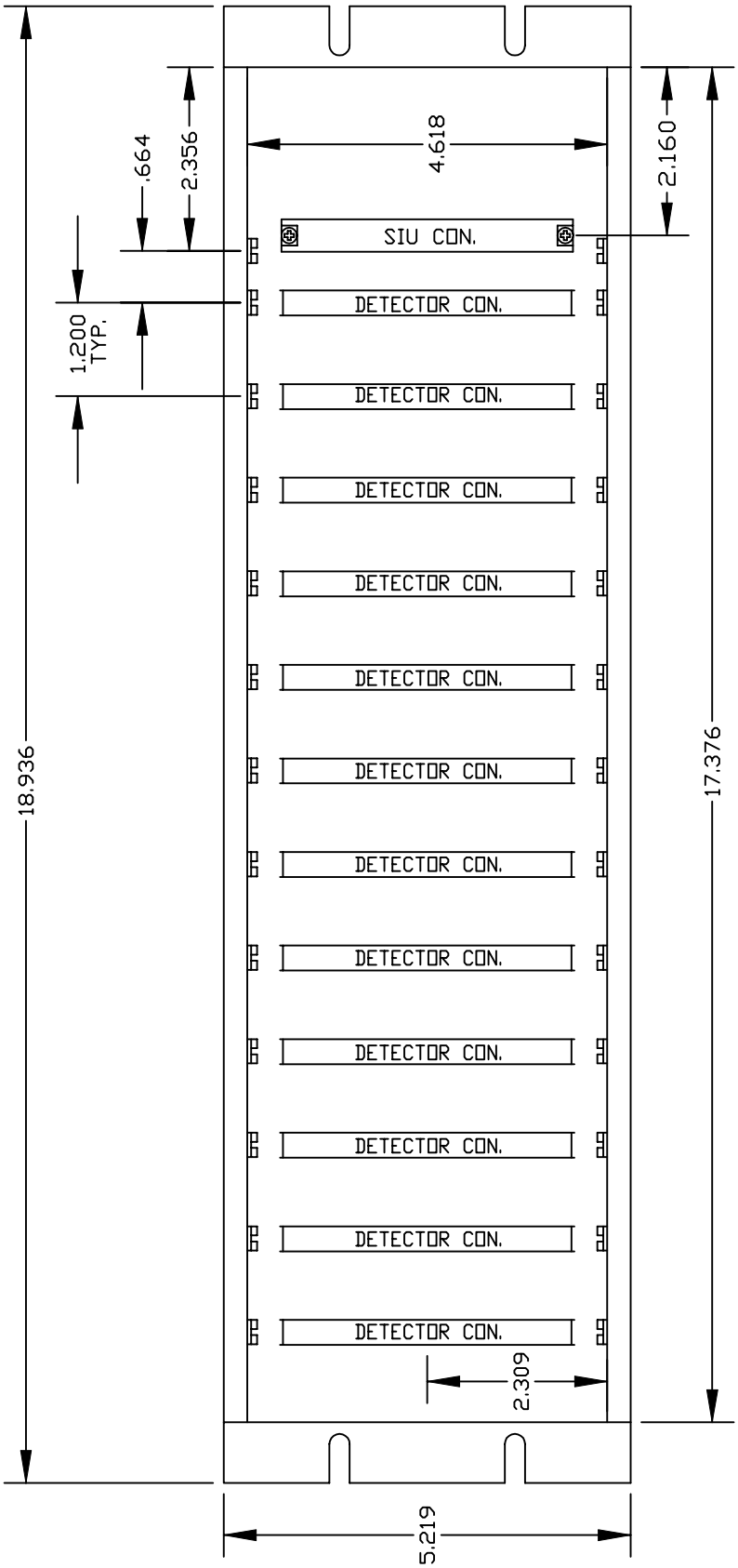
HEAVY DUTY (HD) RELAY SOCKET DETAIL



REAR VIEW

PIN	FUNCTION
1	COIL
2	COIL
3	N.C. CIRCUIT #1
4	N.C. CIRCUIT #2
5	COMMON CIRCUIT #1
6	COMMON CIRCUIT #2
7	N.O. CIRCUIT #1
8	N.O. CIRCUIT #2

TITLE: 6/14 PACK OUTPUT ASSEMBLY FLASHER DIAGRAM	
NO SCALE	7–5–34
MARCH 29, 2002	



TITLE:

INPUT ASSEMBLY FRONT VIEW

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MARCH 29, 2002

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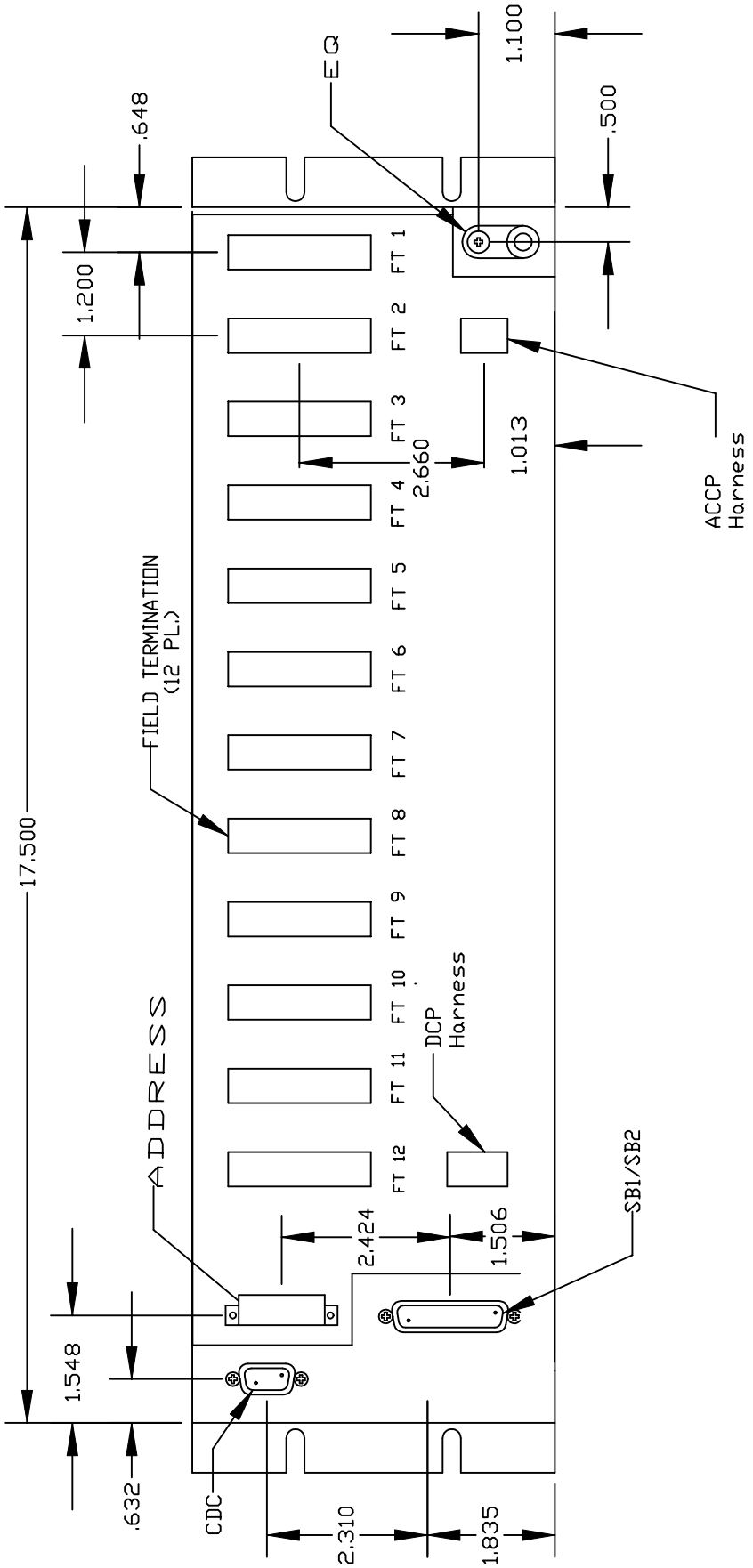

TITLE:	
INPUT ASSEMBLY REAR VIEW	
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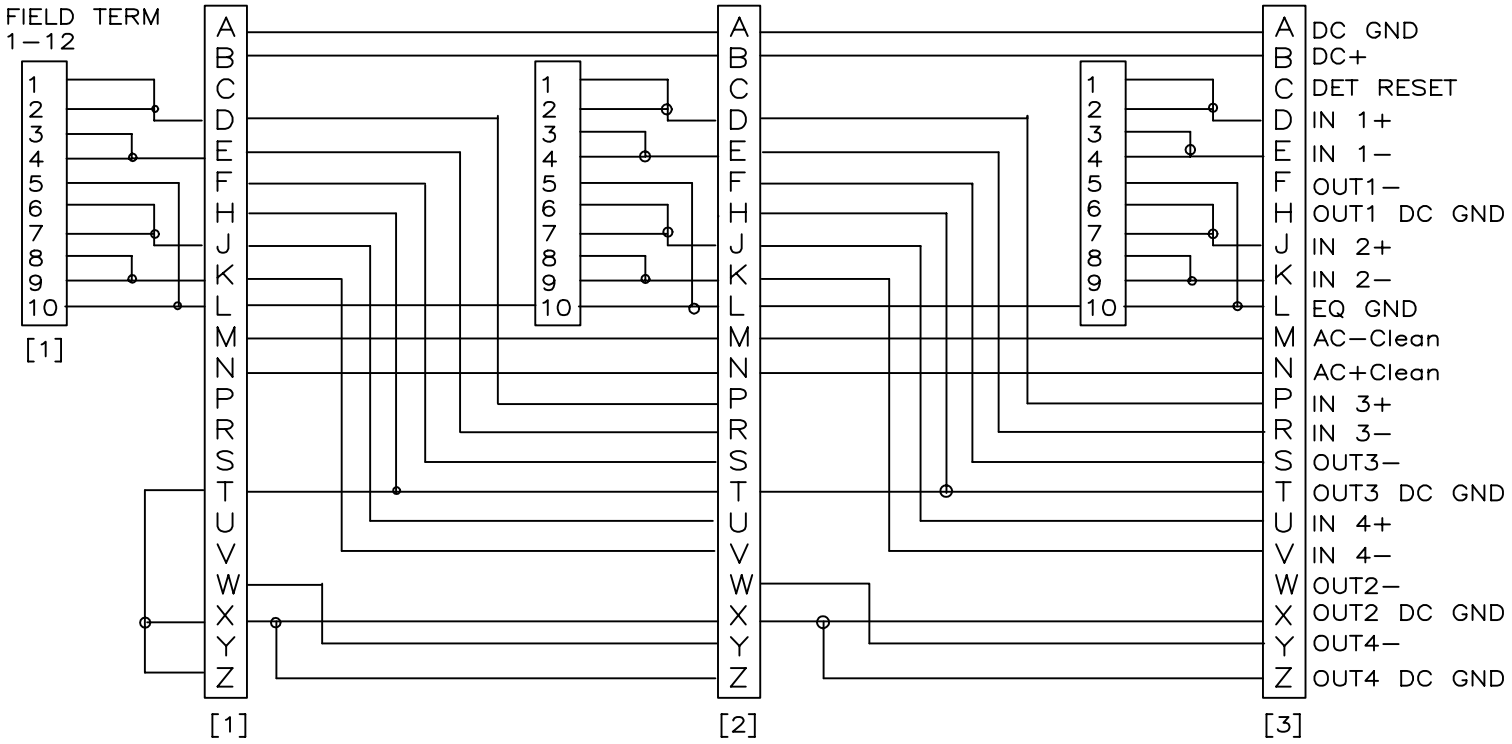
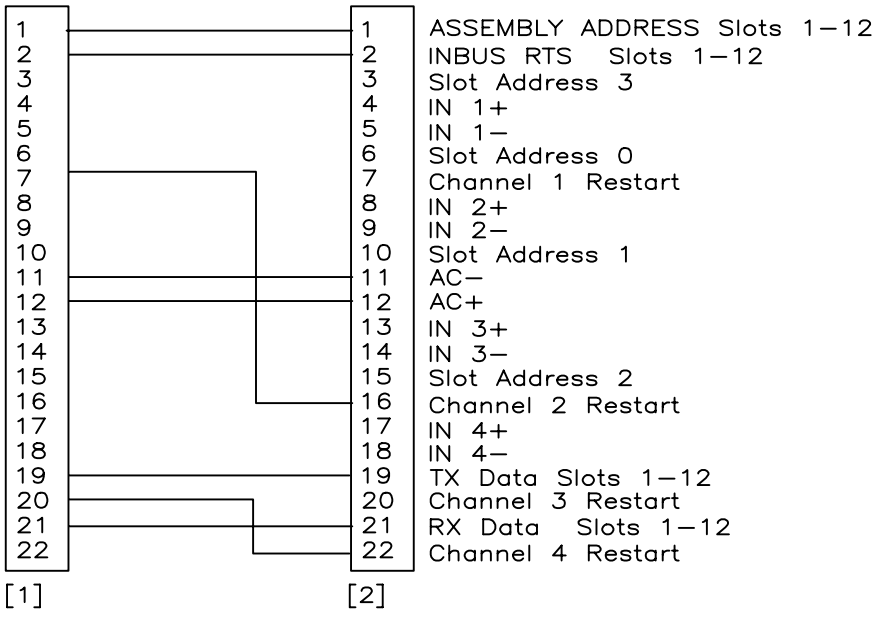
SLOTS 1–12



FIELD INPUT LETTERED SIDE

NUMBERED SIDE of Slots 1–12



FIELD INPUT CONNECTOR NUMBERED SIDE

TITLE:

INPUT ASSEMBLY WIRING DIAGRAMS

NO SCALE

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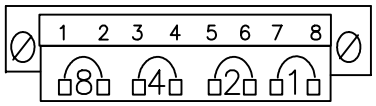
INPUT ASSEMBLY SIU PIN ASSIGNMENTS

PIN	SIU ROW A	SLOT1–12 PINS	SIU ROW B	SLOT1–12 PINS	SIU ROW C	SLOT1–12 PINS
1	+24 in		+24 in	+24 in	I/O 48	Slot 9–20
2	I/O 1	Slot 1–2C	I/O 2	Slot 3–4C	I/O 49	Slot 10–7
3	I/O 3	Slot 5–6C	I/O 4	Slot 7–8C	I/O 50	Slot 10–20
4	I/O 5	Slot 9–10C	I/O 6	Slot 11/12C	I/O 51	Slot 11–7
5	I/O 7	Slot 1F	I/O 8	Slot 1W	I/O 52	Slot 11–20
6	I/O 9	Slot 2F	I/O 10	Slot 2W	I/O 53	Slot 12–7
7	I/O 11	Slot 3F	I/O 12	Slot 3W	I/O 54	Slot 12–20
8	I/O 13	Slot 4F	I/O 14	Slot 4W	SB1 TxD +	Com 2 RXD+
9	I/O 15	Slot 5F	I/O 16	Slot 5W	SB1 TxD –	Com15 RXD–
10	I/O 17	Slot 6F	I/O 18	Slot 6W	SB1 RxD +	Com 1 TXD+
11	I/O 19	Slot 7F	I/O 20	Slot 7W	SB1 RxD –	Com14 TXD–
12	I/O 21	Slot 8F	I/O 22	Slot 8W	SB1 TxC +	Com 4 RXC+
13	I/O 23	Slot 9F	I/O 24	Slot 9W	SB1 TxC –	Com17 RXC–
14	I/O 25	Slot 10F	I/O 26	Slot 10W	SB1 RxC +	Com 3 TXC+
15	I/O 27	Slot 11F	I/O 28	Slot 11W	SB1 RxC –	Com16 TXC–
16	I/O 29	Slot 12F	I/O 30	Slot 12W	LINE SYNC. +	Com 9 LSync+
17	I/O 31	Slot 1–7	I/O 32	Slot 1–20	LINE SYNC. –	Com22 LSync–
18	I/O 33	Slot 2–7	I/O 34	Slot 2–20	N RESET +	Com10NRESET+
19	I/O 35	Slot 3–7	I/O 36	Slot 3–20	N RESET –	Com23NRESET–
20	I/O 37	Slot 4–7	I/O 38	Slot 4–20	ASSY ADDR	Slots1–12(1)
21	I/O 39	Slot 5–7	I/O 40	Slot 5–20	INBUS RTS	Slots1–12(2)
22	I/O 41	Slot 6–7	I/O 42	Slot 6–20	SB2 TxD +	Com 6 RXD+
23	I/O 43	Slot 7–7	I/O 44	Slot 7–20	SB2 TxD –	Com19 RXD–
24	I/O 45	Slot 8–7	I/O 46	Slot 8–20	SB2 RxD +	Com 5 TXD+
25	I/O 47	Slot 9–7	Opto In1	CDC–1	SB2 RxD –	Com18 TXD–
26	Opto In 2	CDC–2	Opto In 3	CDC–3	SB2 TxC +	Com 8 RXC+
27	Opto In 4	CDC–4	OptoComon	CDC–5	SB2 TxC –	Com21 RXC–
28	Address–0	ADC –1	Address–1	ADC –3	SB2 RxC +	Com 7 TXC+
29	Address–2	ADC –5	Address–3	ADC –7	SB2 RxC –	Com20 TXC–
30	INBUS TxD	Slots1–12(21)	INBUS RxD	Slots1–12(19)	SB2 INBUS TXC	NA
31	EQ GND		AC Line Ref	TC 31	SB2 INBUS RxC	NA
32	DC GND		DC GND		SIU ENABLE	SIU 24VDCGND

ADDRESS PLUG

TOP VIEW



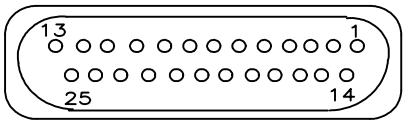
ASSEMBLY	ADDR	ADDR PLUG 8-4-2-1
Input Assembly 1	09	1001
Input Assembly 2	10	1010
Input Assembly 3	11	1011
Input Assembly 4	12	1100
Input Assembly 5	13	1101

Jumper settings are ground true.
Install jumper for logic 1.

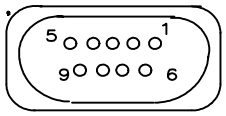
ADDRESS CONNECTOR DETAIL

Pin #	FUNCTION	Pin #	FUNCTION
1	Address 8	2	DC GROUND
3	Address 4	4	DC GROUND
5	Address 2	6	DC GROUND
7	Address 1	8	DC GROUND

COM
SB1/SB2
(Socket Face View)



CDC
(Socket Face View)



COM SB1/SB2 CONNECTOR

Pin	AT THE CONTROLLER	AT THE SIU	Pin	AT THE CONTROLLER	AT THE SIU
1	SB1 TXD+	SB1 RXD+	14	SB1 TXD–	SB1 RXD–
2	SB1 RXD+	SB1 TXD+	15	SB1 RXD–	SB1 TXD–
3	SB1 TXC+	SB1 RXC+	16	SB1 TXC–	SB1 RXC–
4	SB1 RXC+	SB1 TXC+	17	SB1 RXC–	SB1 TXC–
5	SB2 TXD+	SB2 RXD +	18	SB2 TXD–	SB2 RXD–
6	SB2 RXD+	SB2 TXD +	19	SB2 RXD–	SB2 TXD–
7	SB2 TXC+	SB2 RXC+	20	SB2 TXC–	SB2 RXC–
8	SB2 RXC+	SB2 TXC+	21	SB2 RXC–	SB2 TXC–
9	LINE SYNC+	LINE SYNC+	22	LINE SYNC–	LINE SYNC–
10	NRESET+	NRESET+	23	NRESET–	NRESET–
11	PWR DWN+		24	PWR DWN–	
12	+5VDC ISO		25	EQ GND	
13	ISO GND				

CDC (Cabinet DC signal interconnect)

Pin #	FUNCTION	Pin #	FUNCTION
CDC–1	OPTO INPUT 1	CDC–2	OPTO INPUT 2
CDC–3	OPTO INPUT 3	CDC–4	OPTO INPUT 4
CDC–5	OPTO INPUT COMMON	CDC–6	Spare
CDC–7	Spare	CDC–8	Spare
CDC–9	Spare		

TITLE:

INPUT ASSEMBLY CONNECTORS

NO SCALE

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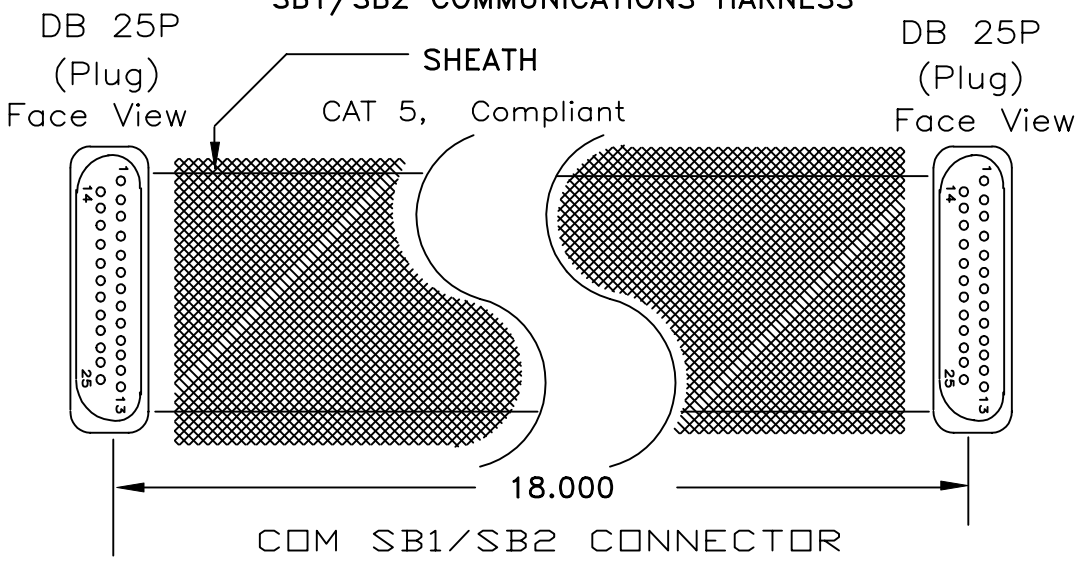
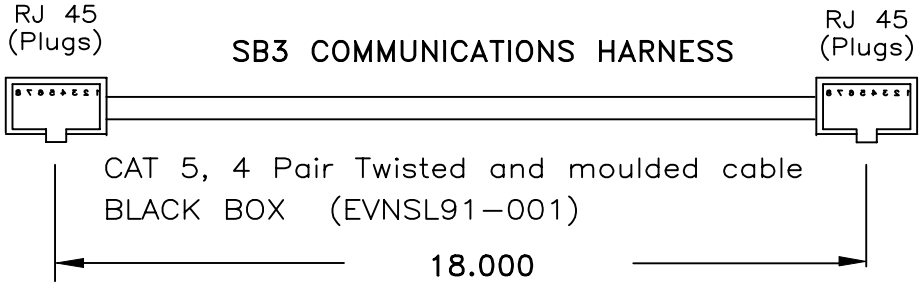
SB1/SB2 COMMUNICATIONS HARNESS



COM SB1/SB2 CONNECTOR

Pin	AT THE CONTROLLER	AT THE SIU	Pin	AT THE CONTROLLER	AT THE SIU
1	SB1 TXD+	SB1 RXD+	14	SB1 TXD−	SB1 RXD−
2	SB1 RXD+	SB1 TXD+	15	SB1 RXD−	SB1 TXD−
3	SB1 TXC+	SB1 RXC+	16	SB1 TXC−	SB1 RXC−
4	SB1 RXC+	SB1 TXC+	17	SB1 RXC−	SB1 TXC−
5	SB2 TXD+	SB2 RXD +	18	SB2 TXD−	SB2 RXD−
6	SB2 RXD+	SB2 TXD +	19	SB2 RXD−	SB2 TXD−
7	SB2 TXC+	SB2 RXC+	20	SB2 TXC−	SB2 RXC−
8	SB2 RXC+	SB2 TXC+	21	SB2 RXC−	SB2 TXC−
9	LINE SYNC+	LINE SYNC+	22	LINE SYNC−	LINE SYNC−
10	NRESET+	NRESET+	23	NRESET−	NRESET−
11	PWR DWN+		24	PWR DWN−	
12	+5VDC ISO		25	EQ GND	
13	ISO GND				

SB3 COMMUNICATIONS HARNESS



SB3 CONNECTOR

Pin #	PAIR COLOR	AT THE PDA	AT THE OUTPUT ASSEMBLY
1	WHITE ORANGE	SP3 TXC+	SP3 RXC+
2	ORANGE	SP3 TXC−	SP3 RXC−
3	WHITE GREEN	AC− RAW	AC−RAW
4	BLUE	SP3 TXD+	SP3 RXD+
5	WHITE BLUE	SP3 TXD−	SP3 RXD−
6	GREEN	AC−RAW	AC−RAW
7	WHITE BROWN	SP3 RXD+	SP3 TXD+
8	BROWN	SP3 RXD−	SP3 TXD−

SERIAL BUS HARNESSES

NO SCALE

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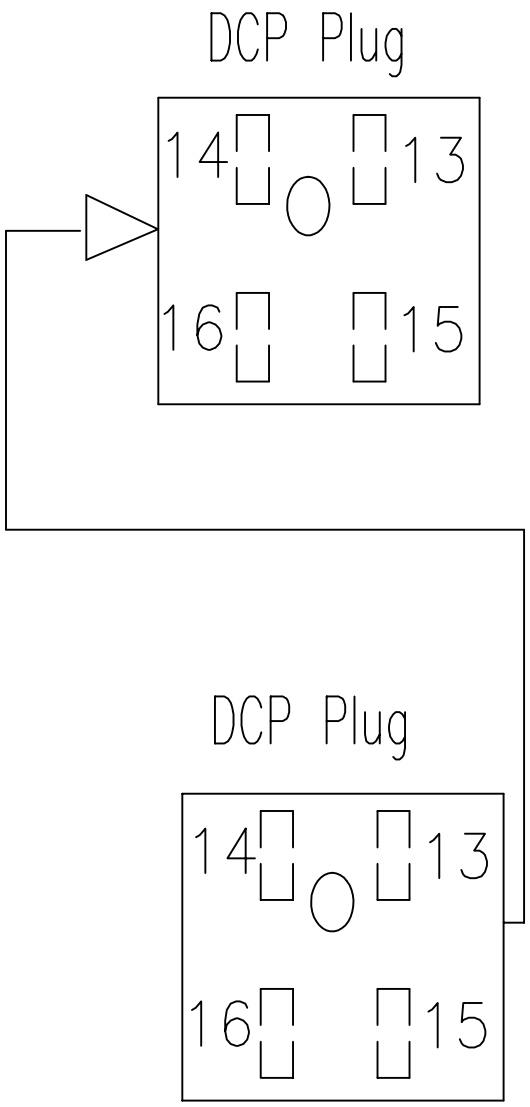

NOTES:

Two BEAU P5404-LAB wired Parallel with #14 gauge minimum wire size. Cable length with connectors shall be 18 inches minimum. Cable ends shall be covered with Rt Angle cable clamp ends. The cable shall be protected.

DCP HARNESS	
NO SCALE	7-5-40
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CHAPTER 9

SPECIFICATION FOR MODEL 2070

CONTROLLER UNIT

TABLE OF CONTENTS

CHAPTER 9 SECTION 1

GENERAL

9.1.1
The Controller Unit shall be composed of the UNIT CHASSIS, modules and assemblies per their version. The following is a list of 2070 Versions, their interface rolls and composition:

UNIT VERSION	DESCRIPTIVE
2070V UNIT	Provides directly driven VME and mates to 170 & ITS cabinets. It consists of: Unit CHASSIS, 2070-1A TWO BOARD CPU, 2070-2A F I/O, 2070-3A FRONT PANEL, 2070-4A POWER SUPPLY, and 2070-5 VME CAGE ASSEMBLY.
2070L UNIT	LITE Unit mates to the 170 & ITS cabinets. It consists of: UNIT CHASSIS, 2070-1B CPU, 2070-2A (2B if ITS CABINET), F I/O, 2070-3B FRONT PANEL and 2070- 4A or B POWER SUPPLY
2070LC UNIT	LITE unit mates to ITS cabinets only. It consists of: UNIT CHASSIS, 2070-1B CPU, 2070-2B F I/O, 2070-3C FRONT PANEL and 2070-4 A or B POWER SUPPLY

- **See Chapter 11 for 2070 NEMA Versions**

9.1.2
The communications and option modules shall be called out separately from the unit version. The composition weight shall not exceed 25 pounds.

9.1.3
The CHASSIS top and Bottom, Internal Structure Supports, Back Plane Mounting Surface, Module Plates, Power Supply Enclosure, and Front Panel shall be made of 63 gauge minimum aluminum sheet. The CHASSIS Side panels shall be 80-gauge minimum sheet

9.1.4
It is noted that the Power Failure Power Restoration operations of this unit are specific to the requirements of the user. All associated modules shall comply to said operations.

9.1.5
2070 UNIT module / assembly power limitations shall be as follows:

Models	+5VDC	+12VDC iso	+12VDC ser	-12 VDC ser
MCB	750 mA	-----	-----	-----
TRANS BD	750 mA	-----	-----	-----
2070-2A FI/O	250 mA	750 mA	-----	-----
2070-2B FI/O	250 mA	500 mA	-----	-----
2070-3A&B FPA	500 mA	-----	50 mA	50 mA
2070-3C FPA	100 mA	-----	50 mA	50 mA
2070-5 VME Cage	5.0 A	-----	200 mA	200 mA
2070-6 All Comm	500 mA	-----	100 mA	100 mA
2070-7 All Comm	250 mA	-----	50 mA	50 mA

9.1.6
All circuitry associated with the EIA-485 Communications links shall be capable of reliably passing a minimum of 1.0 Mbps. Isolation circuitry shall be by opto- or capacitive-coupled isolation technologies.

9.1.7
The EIA-485 Line Drivers/Receivers shall be socket mounted or Surface mounted and shall not draw more than 35 mA in active state and 20 mA in inactive state. A 100-Ohm Termination Resistor shall be provided across each Differential Line Receiver Input. The MOTHERBOARD's control signals (e.g., SP1-RTS) shall be active, or asserted, when the positive terminal (e.g., SP1-RTS+) is a lower voltage than its corresponding negative terminal (e.g., SP1-RTS-). A control signal is inactive when its positive terminal voltage is higher than its negative terminal. Receive and transmit data signals shall be read as a "1" when the positive terminal's (e.g., SP1-TXD+) voltage is higher than its corresponding negative terminal (e.g., SP1-TXD-). A data value is "0" when its positive terminal's (e.g., SP1-TXD+) voltage is lower than its negative terminal (e.g., SP1-TXD-).

9.1.8
Sockets for devices (called out to be socket mounted) shall be "xx" pin AUGAT 500/800 series AG10DPC or equal.

9.1.9
SP5 and SP3 SDLC frame address assignments (Command/Response) are as follows:

	SP 5	SP3
CPU 2070-1	“ 19"	“19”
FI/O 2070-2A	" 20"	“NA”
CPU Broadcast to all	"127"	“255”

All other addresses are reserved by the AGENCY with the exception of NEMA TS2 Type 1 Requirements (See Chapter 11). The SDLC response frame address shall be the same address as the Command frame it receives.

CHAPTER 9 SECTION 2

MODEL 2070-1 CPU MODULE

9.2.1
The MODEL 2070-1A CPU shall consist of the Main Controller Board, Transition Board, Board Interface Harness, and CPU Module Software.

9.2.2
The MODEL 2070-1B CPU shall be a single board module meeting the 2X WIDE Board requirements. The module shall be furnished normally resident in the MOTHERBOARD Slot A5. The module shall meet all the requirements listed under this section and Chapter Details Section 7 except for the following:

9.2.2.1
The VME software and hardware bus requirements shall not apply nor do the MCB and Board Interface Harness physical requirements.

9.2.2.2
A Dual SCC Device (asynch / synch) and associated circuitry shall be furnished to provide two additional system serial ports. The Dual SCC1 shall be assigned to the System Serial Port SP1 meeting all requirements called out for SP1. The Dual SCC2 shall be assigned as System Serial Port SP8. The SP8 and associated circuitry shall interface with the MC68360 address and data structure and serially be connected to the external world via the DB 25 Pin C13S Connector located on the module front panel. The SP8 shall meet all SP2 Port requirements including EIA 485 drivers / receivers and synchronous bps rate of 614 Kbps. An internal LOGIC Switch shall be provided to disconnect SP8 RTS, CTS and DCD (Pins 5, 6,7,18,19 and 20) lines from C13S Connector.

9.2.2.3
The 68360 SCC1 shall be reassigned to ETHERNET (ENET) Network meeting ETHERNET 10 MBPS IEEE 802-3 (TP) 10 BASE T Standard Requirements, both hardware and software. The four network lines shall be used to route ETHERNET across the MOTHERBOARD to the "A" Connectors. DC Grounding plane around the network connectors and lines shall be provided. Network Lines shall be assigned as: Network 1 = ENET TX+, Network 2 = ENET TX-, Network 3= ENET RX+, and Network 4 = ENET RX-. In addition, the conditioned ETHERNET shall be brought out on RJ 45 C14S Connector mounted on the CPU-1B Front Panel. Four LEDs labeled "TX, RX, TX Collision, and TX Status" shall be mounted on the front panel signifying ETHERNET operational conditions.

9.2.2.4
The 2070-1B CPU shall not draw more than 1.25 A of +5VDC & 500 mA of ISO+12 VDC.

9.2.3 MAIN CONTROLLER BOARD (MCB)

9.2.3.1
The MCB shall be a 3U VME bus compliant board and contain a system controller, an A24-D16 interface, a Master & Slave bus interface, a Multilevel VMEbus Arbiter, a FAIR VMEbus Requester and BTO (64).

9.2.3.2
The CONTROLLER Device shall be a Motorola MC68360 or equal, clocked at 24.576 MHz minimum. The Fast IRQ Service System is reserved for State use only. The Interrupts shall be configured as follows:

Level 7 - VMEbus IRQ7, AC FAIL
Level 6 - VMEbus IRQ6
Level 5 - VMEbus IRQ5, CPU Module Counters / Timers, LINESYNC (auto vectored), Serial Interface Interrupts
Level 4 - VMEbus IRQ4
Level 3 - VMEbus IRQ3
Level 2 - VMEbus IRQ2
Level 1 - VMEbus IRQ1

9.2.3.3 MEMORY ADDRESS ORGANIZATION

8000 0000 - 80FF FFFF	**STANDARD**
9000 0000 - 9000 FFFF	**SHORT**

9.2.3.3.1
16 megabytes of contiguous address space for each specified memory (DRAM, SRAM and FLASH) shall be allocated on an even boundary. The SRAM and FLASH memories shall be accessed through the OS-9 Operating System's supplied file Manager.

9.2.3.3.2
When the incoming +5 VDC falls below its operating level, the SRAM shall drop to its standby state and the SRAM and TOD Clock shall shift to the +5 VDC Standby Power. A on-board circuit shall sense the +5 VDC Standby Power and shift to a On-board CPU Power source. The CPU On-board Power shall be capable of holding the SRAM and TOD Clock up for 30 Days. When the incoming +5 VDC rises to within its operating level, the appropriate MCB Circuitry shall shift from standby power to incoming +5 VDC.

9.2.3.4 RAM MEMORY
A minimum of 4 MB of DRAM, organized in 32-bit words, shall be provided. A minimum of 512 KB of SRAM, organized in 16 or 32-bit words, shall be provided. The time from the presentation of valid RAM address, select lines, and data lines to the RAM device to the acceptance of data by the RAM device shall not exceed 80 ns and shall be less as required to fulfill zero wait state RAM device write access under all operational conditions.

9.2.3.5 FLASH MEMORY
A minimum of 4 MB of FLASH Memory, organized in 16-bit or 32-bit words, shall be provided. The MCB shall be equipped with all necessary circuitry for writing to the

FLASH Memory under program control. No more than 1 MB of FLASH Memory shall be used for Boot Image (List) and a minimum of 3 MB shall be available for AGENCY use.

9.2.3.6 TIME-OF-DAY CLOCK

A software settable hardware Time-of-Day (TOD) clock shall be provided. It shall under on-board standby power, operate for a minimum of 30 days maintaining an accuracy of ±1 minute per 30 days at 25° C. The clock shall be alined to a minimum fractional second resolution of 10 ms and shall track seconds, minutes, hours, day of month, month, and year.

9.2.3.7

A software-driven CPU RESET signal (Active LOW) shall be provided to reset other controller systems. The signal output shall be driver capable of sinking 30 mA at 30 VDC. Execution of the program module "CPURESET" in the boot image shall assert the CPU RESET signal once.

9.2.3.8

An open-collector output, capable of sinking 30 mA at 30 VDC, shall be provided to drive the Front Panel Assembly CPU Activity LED INDICATOR.

9.2.3.9*

The OS-9 Operating System TICK Timer shall be derived from the each transition of LINESYNC with a tick rate of 120 ticks per second.

9.2.3.10

The SRAM and TOD Clock Circuitry under Standby mode shall draw no more than 8uA at 2.5 VDC and 35 degrees C. A On board Capacitor supply shall hold up SRAM and TOD for a minimum of 7 days. The +5VDC Standby Power shall hold up the SRAM and TOD Circuitry while CPU is resident in 2070 (31 Days).

9.2.4*

A TRANSITION Board (TB) shall be provided to transfer serial communication and control signals between the MCB and the Interface Motherboard. Said signal and communication lines shall be driven/received off and on the module compliant to EIA- 485. The Transition Board shall provide a 1 K-Ohm pull-up resistor for the A2 &A3 INSTALLED lines. If the DC Ground is not present (slot not occupied) at the CPU EIA-485 line drivers/receivers, the drivers/receivers shall be disabled (inactive).

9.2.5

A SHIELDED INTERFACE HARNESS shall be provided. It shall include MCB and Transition Board connectors with strain relief, lock latch, mating connectors, and harness conductors. A minimum of 25 mm of slack shall be provided. No power shall be routed through the harness. The harness shall be 100% covered by an aluminum mylar foil and an extruded black 0.8 mm PVC jacket or equal.

9.2.6 DATA KEY

A DATAKEY Keyceptacle™ (KC4210, KC4210PCB or equal) with Key shall have minimum 16 kbit Datakey™ P/N 611-0070-000 (BLACK) resident and mounted on the CPU

module front panel (or the Transition Board of Model 1A). The serial memory key shall be temperature rated for –40 to +80 °C operation. The Black DATAKEY shall be tested, interrogated and all 128 addresses read using Software Interface. Power shall not be applied to the receptacle if the key is not present.

The memory is reserved by the Agency. Capability to program the DATAKEY shall be provided by the contractor.
A Utility Program shall be provided that reads the DATAKEY for an IP Address, Network Netmask and Default Gateway. This Utility Program shall set the IP Address, Network Netmask and Default Gateway of the Model 2070 Controller when executed by a user at the command line or via a standard OS-9 startup file.

9.2.7 CPU MODULE SOFTWARE

The following shall be supplied:

1. **Operating System**
2. **Drivers and Descriptors**
3. **Application Kernel**
4. **Error Handler**
5. **Validation Suite**
6. **Deliverables**

9.2.7.1 OPERATING SYSTEM

The CPU Module shall be supplied with Microware Embedded OS-9 Version 3.2 or later software and, in addition, the following:

1. **Embedded OS-9 Real Time Kernel**
2. **Sequential Character File Manager (SCF)**
3. **Sequential Protocol File Manager (SPF)**
4. **Pipe File Manager (PIPEMAN)**
5. **Random Block File Manager (RBF)**
6. **C Shared Library (CSL)**

Boot Image shall include the following utility modules:

Break	**Date**	**Deiniz**	**Devs**	**Free**	**Copy**
Dir	**Tmode**	**Edt**	**List**	**Load**	**Deldir**
Dump	**Del**	**Ident**	**Iniz**	**Irqs**	**Events**
Echo	**Csl**	**Dcheck**	**Login**	**Link**	**Kermit**
Tsmon	**Mdir**	**Mfree**	**Pd**	**Makdir**	**Save**
Attr	**Rename**	**Procs**	**Unlink**	**Sleep**	**Xmode**
Shell	**Build**	**Setime**	**Format**		

9.2.7.2 DRIVERS AND DESCRIPTORS

9.2.7.2.1
Supplied modules shall be re-entrant, address independent, and shall not contain self-modifying code.

Device drivers which require extensions to the standard Microware libraries shall use the _os_getstat() and _os_setstat() functions as follows:

A custom setstat code and parameter structure are defined thus:

```
#define SS_2070       0x2070

error_code _os_getstat(path_id path, SS_2070, void *pb);
error_code _os_setstat(path_id path, SS_2070, void *pb);

typedef struct
{
     u_int32 code;
     u_int32 param1;
     union
     {
          u_int32 param_2070;
          void    *pb_2070;
     } param2;
} pb;
```

Note: For OS-9 68K, the _os_getstat() and _os_setstat() functions are in the conv_lib.l file.

9.2.7.2.2
Drivers shall be provided to access the FLASH, SRAM, and DRAM memories. The following descriptors shall apply:

/d0	**Floppy Diskette Drive**	**Reserved name; no driver required**
/f0	**FLASH Drive**	**Accessed as RAM disk & OS-9 /dd default Device**
/f0wp	**FLASH Drive**	**Same as /f0 but, write protection**
/f0fmt	**FLASH Drive**	**Same as /f0 except format enabled**
/h0	**Hard Disk Drive**	**Reserved name; no drive required**
/r0	**SRAM Drive**	**Accessed as RAM disk**
/r0fmt	**SRAM Drive**	**Same as /r0 except format enabled**
/r1		**Reserved; no driver required**
/r2	**Temporary DRAM Drive**	**Allows 1 MB of DRAM, accessed as RAM disk; not initialized at boot time**

9.2.7.2.3
A driver to handle each of the four internal timers under the OS-9 Kernel shall be provided. Access to the MC68360 internal timers shall be through the following descriptors:

9.2.7.2.3.1

Descriptor names for each timer:

timer1 = access to MC68360's internal timer #1
timer2 = access to MC68360's internal timer #2
timer3 = access to MC68360's internal timer #3
timer4 = access to MC68360's internal timer #4
timer12 = access to MC68360's internal timer #1 & #2 [cascaded]
timer34 = access to MC68360's internal timer #3 & #4 [cascaded]

9.2.7.2.3.2

Timer descriptor option structure:

The driver shall change appropriate functions only and ignore values that do not apply to a particular timer function. The data structures are as follows:

```
struct TER /* timer event register */
{
   unsigned reserveTER     :14;    /* reserved                  */
   unsigned timerREF       :1;     /* output Reference Event    */
   unsigned timerCAP       :1;     /* Capture event             */
};

struct TMR /* timer mode register */
{
   unsigned timerPS        :8;     /* prescale                          */
   unsigned timerCE        :2;     /* capture edge/enable interrupts    */
   unsigned timerOM        :1;     /* output mode                       */
   unsigned timerORI       :1;     /* output reference enable           */
   unsigned timerFRR       :1;     /* free run or restart               */
   unsigned timerICLK      :2;     /* input clock source (Default = 1)  */
   unsigned timerGE        :1;     /* gate enable                       */
};

struct TGCR /* timer global configuration register */
{
   unsigned reserveTGCR    :12;    /* reserved                          */
   unsigned timerCAS_GM    :1;     /* cascade timers / Gate mode        */
   unsigned timerFRZ       :1;     /* freeze timer                      */
   unsigned timerSTP       :1;     /* stop timer                        */
   unsigned timerRST       :1;     /* reset timer                       */
};

typedef struct
{
   union
   {
      struct TGCR TGCR;   /* timer global configuration register */
```

```
    unsigned short tgcr;
  } uTGCR;

  union
  {
    struct TMR  TMR;      /* timer mode register        */
    unsigned short tmr;
  } uTMR;

  u_int32  timerTRR;      /* timer reference register   */
  u_int32  timerTCR;      /* timer capture register (Read Only) */

  union
  {
    struct TER TER;       /* timer event register       */
    unsigned short ter;
  } uTER;

} TTimer_opts;
```

Note:
The maximum timerTRR value for a non-cascaded timer is 0x0000ffff (65535).
The maximum timerTRR value for a cascaded timer is 0xffffffff (4294967295).

9.2.7.2.3.3
Timer Standard OS-9 Function Calls:

error_code _os_open (char *timer_desc_name, path_id *path);

error_code _os_write (path_id path, u_int32 *timer_value, u_int32 *size_timer_write);

Note: Prior to the _os_write() **execution, the u_int32 size_timer_write must be loaded with the value 4.**
error_code _os_read (path_id path, void *timer_read, u_int32 *size_timer_read);

Note: Prior to the _os_read() **execution, the u_int32 size_timer_read must be loaded with the value 4.**

error_code _os_ss_sendsig (path_id path, signal_code timer_sig);

Note: The os_ss_sendsig() **command must be reset each time the signal is sent.**

Note: The driver shall be capable of using a previously set timerTRR value to begin timing upon reception of the os_ss_sendsig() **request without the need for issuing an additional write command.**

error_code _os_ss_relea (path_id path);
error_code _os_close (path_id path);

NOTE:
The following two function calls cannot be used with standard Microware File Managers and the timer structure defined in Section 9.2.7.2.3.2. That structure must be modified to leave room at the beginning of the structure for the predefined standard File Manger storage. This storage is different for each file manager.

error_code _os_gs_popt (path_id path, u_int32 *size_TTimer_opts, void *timer_opts);

Note: Prior to the _os_gs_popt() **execution, the u_int32 size_TTimer_opts must be loaded with the value sizeof(TTimer_opts).**

error_code _os_ss_popt (path_id path, u_int32 size_TTimer_opts, void *timer_opts);

9.2.7.2.3.4
Timer Extension to Standard OS-9 Function Calls:

error_code _os_getstat(path_id path, SS_2070, void *pb);

The timer driver will support the following modes using the SS_2070 _os_getstat() option code and a custom parameter block structure:

Get Timer options (replacement for _os_gs_popt ()).
Use existing standard Microware #define SS_OPT

```
pb.code = SS_OPT;  /* options */
pb.param1 = (u_int32 *) size_TTimer_opts;        /* ptr to struct size variable */
pb.param2.pb_2070 = (struct TTimer_opts) *timer_opts;         /* storage */
```

Note: Prior to the _os_getstat () **execution, the u_int32 size_TTimer_opts variable must be loaded with the value sizeof(TTimer_opts).**
9.2.7.2.3.5
Timer Extension to Standard OS-9 Function Calls:

error_code _os_setstat(path_id path, SS_2070, void *pb);

The timer driver will support the following modes using the SS_2070 _os_setstat() option code and a custom parameter block structure:

a) Set Timer options (replacement for _os_ss_popt ()).

Use existing standard Microware #define SS_OPT

```
pb.code = SS_OPT;  /* options */
pb.param1 = u_int32 size_TTimer_opts;   /* struct size */
pb.param2.pb_2070 = (struct TTimer_opts) *timer_opts; /* ptr to storage */
```

b) Timer Signal Operations - General

The time increment per count shall be initialized to (approximately) 1 uS, unless an _os_setstat() w/ SS_OPT **has set a different value.**

The maximum Timer Reference Register value for a non-cascaded timer is 0x0000ffff (65535). For greater values, cascaded timers /timer12 or /timer34 must be used. In these cases, the independent use of /timer1 and /timer2 or /timer3 and /timer4 is not available when cascaded.

The driver shall perform the necessary action to start (or cancel) the timing process upon receipt of the _os_setstat() request defined below.

The timer shall use the FRR bit set to 1 (Restart) to reset the timer count immediately after the reference value is reached.

Send a signal after specified time interval.

This command must be issued each time the signal is desired to be sent.
#define SS_TIMER_SET 0x1000

```
pb.code = SS_TIMER_SET;          /* provision for one shot signal */
pb.param1 = (signal_code) timer_sig;       /* signal code to send (0 = cancel) */
pb.param2.param_2070 = u_int32 timer_value;   /* specify timerTRR value */
```

Note: The timer driver Interrupt code shall STOP the timer (set STP# to 1).

Send recurring periodic signal.

This command is issued once and the signal is sent at the interrupt interval.

The command to Cancel must be issued to stop the signal.
#define SS_TIMER_CYC 0x1001

```
pb.code = SS_TIMER_CYC;          /* provision for periodic signal */
pb.param1 = (signal_code) timer_sig;       /* signal code to send (0 = cancel) */

pb.param2.param_2070 = u_int32 timer_value;   /* specify timerTRR value */
```

Note: The timer driver Interrupt code shall not STOP the timer.

9.2.7.2.3.6
The minimum allowed timer period shall be related to the Processor execution speed, wherein a 24.576 MHz processor would typically have a range of 400 to 500uS in a repetitive mode. The driver shall return error E$Param should any timer parameters be passed which would lead to a shorter timer period.

> **This restriction is to prevent the system from becoming overloaded with timer interrupts.**

In the "one shot" mode, shorter time periods could be allowed. The bootcode provider must test and determine the low point value where "failure to complete" the function exists. This low point must be valid during high levels of system activity which might induce delay in the Timer IRQ response time.

9.2.7.2.4
The OS-9 SCFMAN shall provide access to the CPU Datakey and its control through the following descriptor name and OS-9 functions:
Descriptor name:
datakey = CPUDatakey

Function Calls:
error_code _os_open (char *datakey_desc_name, path_id *path);
error_code = E$NotRdy if CPUDatakey is not installed

error_code _os_read (path_id path, void *control, u_int32 *data_size);
error_code = E$NotRdy if CPUDatakey is not inserted

Note: Prior to the _os_read() **execution, use _os_gs_ready() to determine the data size actually available [typically, 128 bytes].**

error_code _os_close (path_id path);

9.2.7.2.5
The async-communications serial device driver shall operate in six modes described below to accommodate communications network (EIA 232) and their associated flow control mode number (FCM #).

FCM# Description

0) No Flow Control Mode: The CTS and CD signals are set asserted internally, so the serial device driver can receive data at all times. Upon a write command, the serial device driver asserts RTS to start data transmission, and de-asserts RTS when data transmission is completed. This is the default mode for Model 2070 controllers. When user programs issue the first RTS related command, the driver switches to Manual Flow Control Mode.

1) Manual Flow Control Mode: The serial device driver transmits and receives data regardless of the RTS, CTS, and CD states. The user program has absolute control of the RTS state and can inquire of the states of CTS and CD. The states of CTS and CD are set externally by a DCE. The device driver doesn't assert or de-assert the RTS.

2) Auto-CTS Flow Control Mode: The serial device driver transmits data when CTS is asserted. The CTS state is controlled externally by a DCE. The user program has absolute control of the RTS state. The CD is set asserted internally. The device driver doesn't assert or de-assert the RTS.

3) Auto-RTS Flow Control Mode: The CTS and CD are set asserted internally. The serial device driver receives and transmits data at all times. Upon a write command, the serial device driver asserts RTS to start data transmission, and de-asserts RTS when data transmission is completed. If the user program asserts the RTS, the RTS remains to be on until user program de-asserts RTS. If user program de-asserts RTS before the transmitting buffer is empty, the driver holds RTS on until the transmitting buffer is empty. Parameters related to delays of the RTS turn-off after last character are user configurable.

4) Fully Automatic Flow Control Mode: The serial device driver receives data when CD is asserted. Upon a write command, the serial device driver asserts RTS and wait for CTS, starts data transmission when CTS is asserted, and de-asserts RTS when data transmission is completed. Parameters related to delays of RTS turn-off after last character are user configurable. If user program asserts the RTS, RTS remains to be on until user program de-asserts RTS. If user program de-asserts RTS before the transmitting buffer is empty, the driver holds RTS on until the transmitting buffer is empty.

5) Dynamic Flow Control Mode: The Serial device driver maintains a transmit buffer and a receive buffer with fixed sizes, controls the state of RTS and monitors the state of CTS. The transmission and reception of data are managed automatically by the serial device driver. The serial device driver transmits data when CTS is asserted. The serial device driver asserts RTS when its receiving buffer is filled below certain level (low watermark), and de-asserts RTS when its receiving buffer is filled above certain level (high watermark).

The serial device driver shall be able to accept user configuration commands to configure the device driver via OS9_os_ss_size() function call and to accept user request commands for status of serial port from the device driver via OS9_os_gs_size() function call.

The single 32-bit variable passed by_os_ss_size() is defined as follow:

a) Flow Control Code is SS_OFC (0x23):

Bits Description

31-24	**Auto RTS turn-off extension count in number of characters (range=0-255 1=default).**
15	**Auto RTS turn-off extension timing (0=bps rate=default, 1=equivalent 1200 bps).**
14-13	**Reserve for Future Use (default=0).**
12	**Inhibit Change of SCC MRBLR for opened path (default =0; 0=NO; 1=inhibit).**
11	**Inhibit SCC TODR for opened path (default=0; 0=NO; 1=inhibit).**
10-8	**Flow Control Mode Number (FCM#) (range=0-5).**
7-0	**Flow Control Code (FCC) =0x23**

Note: The RTS turn-off extension can represent a bps rate independent time value rather a number of character times, (higher bps rates are normalized to equivalent 1200 bps characters) when selected by bit 15=1. Thus, a value of 4 represents the time of four characters at 1200 bps even when the actual rate is 9600. If bit 15=0, then an extension value = 4 represents 4 characters, which at a bps rate of 9600 would extend the RTS by approximately 3.3 ms.

b) Flow Control Code is SS_IFC (0x22):

Bits Description

31-22	**Flow Control Mode 5 high water mark value (range=1-1023; default=256).**
21-12	**Flow Control Mode 5 low water mark value (range=1-1023; default=256).**
11	**Inhibit DCD activating control (default=0; 0=off; 1=on).**
10	**DCD flow control is active (default=0; 0=NO; 1=YES, changed by FCM#).**
9-8	**Reserved for Future Use (default=0).**
7-0	**Flow Control Code (FCC) = 0X22.**

Note: The inhibit DCD selection has priority over the DCD ON request in the same access. Therefore, sending 0x0000022 results in DCD inhibit and DCD Flow Control inactive for all Flow Modes. A new flow control mode number shall set DCD function to that required in the new mode unless DCD is inhibit is ON.

c) Flow Control Code is SS-Ssig (0x1a):

Bits Description

31-16	**A signal number to be sent to calling process when the state of a pin is changed.**
15-14	**Reserved for Future Use (default=0).**
13	**Ring is asserted (capable hardware only).**
12	**CTS is de-asserted.**
11	**CTS is asserted.**
10-8	**Reserved for Future Use (default=0).**
7-0	**Flow Control Code (FCC) = 0x1a.**

d) Flow Control Code is SS-DCmd (0x0d):

Bits	Description
31-15	Reserved for Future Use (default=0).
14	De-assert DTR (capable hardware only).
13	Assert DTR (capable hardware only).
12	De-assert RTS (duplicated function with_os_ss_DsRTS();).
11	Assert RTS (duplicated function with_os_ss_EnRTS();).
10-8	Reserved for Future Use (default=0).
7-0	Flow Control Code (FCC)=0x0d.

The single 32-bit variable returned by_os_gs_size() is defined as follow:

Bits	Description
31-16	Current unfilled transmit buffer character count of the serial device driver.
15-11	Reserved for Future Use (default=0).
10-8	Current Flow Control Mode Number (FCM#).
7	Reserved for Future Used (default=0).
6	Overrun error –0=no error; 1=error on last received character.
5	Frame error –0=no error; 1=error on last received character.
4	Parity error –0=no error; 1=error on last received character.
3	Ring state –0=de-asserted; 1=asserted (capable hardware only).
2	DSR state –0=de-asserted; 1=asserted (capable hardware only).
1	DCD state –0=de-asserted; 1=asserted.
0	CTS state –0=de-asserted; 1=asserted.

9.2.7.2.6
Four input buffering modes shall be provided:

1. **Line - characters are buffered up to and including a programmable termination character.**

2. **Fixed -a fixed specific number of characters is buffered by the driver.**

3. **Timed- characters are buffered until a programmable inter-character time out occurs.**

4. **Raw – characters are unbuffered and delivered to the task as received.**

9.2.7.2.7
Line, Fixed, and Timed Modes shall be capable of being used together. Raw mode shall disable all other buffering modes.

9.2.7.2.8
Device drivers compliant with the OS-9 SCFMAN shall be provided for CPU Activity LED Indicator and Day Light Savings time correction features. The descriptor names shall be as follows:

led = access to CPU Activity LED Indicator
dstclock = access to Daylight Savings Time Clock correction

The standard OS-9 SCFMAN library calls and their functions are as follows:

```
error_code  _os_open (char *desc_name, path_id *path);     //open descriptor for command
error_code  _os_close (path_id path);                      //close descriptor
error_code  _os_write (path_id path, void *value, 1);      //set value or function
        *value = 1, turn led on or turn DLSclock feature on (default)
        *value = 0, turn led off or turn DLSclock feature off
error_code  _os_read (path_id path, void *value, 1);       //get current state
```

9.2.7.2.9
TIME OF DAY (TOD) CLOCK - The OS-9 operating system's TOD Clock shall be driven by the LINESYNC derived OS-9 Operating System TICK Timer. The manufacturer shall provide the following features to support the TOD operation and synchronization.

9.2.7.2.9.1
Leap Year and Daylight Savings Time (DST) Adjustments - The OS-9 System clock / calendar shall automatically be adjusted to account for DST and leap years. A SCFMAN driver shall be provided to enable/disable the automatic DST adjustment.

9.2.7.2.9.2
Setting Hardware Clock from OS-9 System Clock - A device driver compatible with the OS-9 SCFMAN shall be provided to allow the hardware TOD clock/calendar to be updated from the OS-9 system clock under application control. The descriptor name shall be "ClockUpdate." Opening the descriptor shall cause the driver to synchronize the clock to a minimum of 10 ms resolution. The driver shall compensate for any time elapsed during the process of updating the hardware clock.

9.2.7.2.9.3
Setting OS-9 System Clock from Hardware Clock - At system power up, the OS-9 system TOD clock/calendar shall automatically be updated from the hardware TOD clock. The clocks shall by synchronized to a minimum of 10 ms resolution.

9.2.7.2.10
The FLASH RAM drive (/f0) shall be protected from corruption due to power failure during a write operation. The current sector of FLASH being written shall first be backed up in SRAM. The backup sector copy shall be invalidated when FLASH write operation is completed. In case of power failure, the FLASH driver shall detect the presence of the valid backup sector copy in SRAM and shall read sector data from the valid backup sector copy. A user write operation shall restore the valid backup sector copy first. Execution of the

program module, "FLRESTORE," in the Boot Image shall also restore the valid backup sector copy to FLASH drive after a specified delay. "FLRESTORE" shall accept a delay parameter in seconds ranging from 0 to 600 seconds. The default delay factor is 30 seconds. No more that 150 KB of SRAM shall be dedicated to this purpose. A large file being written, but truncated due to power fail, shall not be restored intact.

9.2.7.2.11 NETWORK REQUIREMENTS

The following OS-9 modules should be included in the /f0/CMDS/BOOTOBJS flash disk directory to allow for standard TCP/IP network communications using Ethernet Protocol over Ethernet hardware and/or Serial Line Internet Protocol (SLIP) or Point-to-Point Protocol over serial links:

1. **OS-9 SPF Ethernet hardware driver and descriptor for 68360 (SCC1) on 2070-1B Controller.**
2. **Drivers and Descriptors for PPP for the 68360.**
3. **Drivers and Descriptors for SLIP for the 68360.**
4. **LAN Comm Pak modules: spenet, enet, spip, ip0, sptcp, tcp0, spudp, udp0, spraw, raw0, sproute, route0, spipcp, ipcp0, splcp, lcp0, sphdlc, hdlc0, spslip, sps10**
5. **Network modules pkman, pkdvr, pk, pks**
6. **Network Trap Handler: netdb_local, netdb_dns**
7. **NFS Modules: nfs, nfsnul and nfs_devices.**

The following Network utilities shall be included and shall reside in the /f0/CMDS directory as identified in this specification.

ftp, ftpdc, idbdump, idbgen, ifconfig, dhcp, inetd, ipstart, ndbmod, netstat, ping , route, telnet, telnetdc, and hostname, nfsc, mount, rpcdump, nfsstat, exportfs, portmap, nfsd, mountd and showmount.

Multi-user functionality

The boot image init module shall be configured with a "default directory name" as /f0wp. This will be allow login and tsmon to provide the user with login prompt from the terminal port or from the network via a telnet session.

The following OS-9 modules should be included in the flash boot image for the implementation of multi-user mode.

login, tsmon

Network Configuration at boot up.

Factory built inetdb, inetdb2 and rpcdb shall reside in the directory /f0/CMDS/BOOTOBJS

Standard Microware File System Configuration

The 2070 shall follow Standard Microware File System Configuration. A /f0/CMDS, /f0/CMDS/BOOTOBJS and /f0/SYS directories should be implemented. The /f0/CMDS directory shall contain the network modules mentioned above as well any other modules not part of the OS9boot image. Execute permission shall be included in the attributes of files in the /f0/CMDS directory. Sysgo should set its execution directory to /f0wp/CMDS prior to spawning opexec or other processes. The /f0/CMDS/BOOTOBJS shall contain the modules as identified above and other customizable descriptors and modules. The /f0/SYS should contain a "password" file. The password file should follow Microware's password file format for the addition and configuration of multi-user functionality and password protection. A user name "super" with password as "user" shall be defined in the password file.

9.2.7.3 APPLICATION KERNEL

9.2.7.3.1
The provided software shall boot OS-9 from SYSRESET. The entire program shall be resident in FLASH Memory. The initialization routines shall configure the serial port protocols as follows:

SP1 & 2	**1.2 Kbps, 8-bit word, 1 stop, no parity, no pause, no echo**
SP 3S	**614.4 Kbps**
SP4	**9.6 Kbps, 8-bit word, 1 stop, no parity, no pause, x on and x off BOTH OFF**
SP 5S	**614.4 Kbps**
SP 6	**38.4 Kbps, 8-bit word, 1 stop and no parity**

9.2.7.3.2
Hardware initialization, preliminary self-test, OS-9 initialization (except Extended Memory Test), and forking OPEXEC shall be completed in less than 1.3 seconds.

9.2.7.3.3
A Trap Library routine, "Warmboot," shall be provided, which upon execution shall first shut down the OS-9 operating system, then jump to the start of the initialization routines executed on SYSRESET and proceed.

9.2.7.3.4
After initialization (boot up from SYSRESET), Sysgo shall fork the defined module in named OPEXEC if present and the backspace key is not pressed on a terminal device attached to /sp4 (c50s). If OPEXEC is not present then Sysgo shall fork a shell that executes a standard OS-9 startup file if present at /f0wp/startup. If startup is not present at /f0/startup then the shell prompt shall be provide on /sp4.

9.2.7.3.5
A Short Out is defined as the period of time between ACFAIL/POWER DOWN transition to LOW and back to HIGH without a SYSRESET transition to LOW. ACFAIL/POWER DOWN transitions shall generate an interrupt. The interrupt shall generate an event

named ACFAIL. The ACFAIL shall have a value 1 indicating an ACFAIL condition has occurred for the DOWN transition and 0 indicating non-ACFAIL condition for the HIGH transition.

A Long Out is defined as ACFAIL transition to LOW follow by a SYSRESET going LOW. The SYSRESET going HIGH shall be followed by an operating system reboot.

9.2.7.4 ERROR HANDLER

9.2.7.4.1
Error handling routine to cope with initialization and power-up test anomalies shall be provided. Errors that occur during initialization and/or during power-up test shall produce a report.

9.2.7.4.2
The Error Handler shall respond to the following conditions and generate an Error Report (saved in Memory):

1. **Timer initialization error**
2. **Timer power up test error**
3. **Serial communication port initialization error**
4. **Serial communication port power up test error**
5. **Peripheral component initialization error**

9.2.7.4.3
The Error Handler error report shall contain, at a minimum, component identification and an error code to identify the form of the error. The error report shall be a file accessible through the Random Block File Manager and named "ErrorReport."

9.2.7.5 VALIDATION SUITE

9.2.7.5.1
A validation suite of software and associated documentation shall be provided. It shall include all diagnostic programs necessary to test all 2070 UNIT functions. The diagnostic programs shall demonstrate that all software and hardware functions operate in conformance to specified functionality. It shall provide a working example of how to program all functions.

9.2.7.5.2
Validation suite software and associated documentation shall be segmented into individual test sequences. It shall be possible to separate out any one or group of these sequences and, with the addition of a general header file, execute it in isolation or in combination with application software.

9.2.7.5.3
When factory boot code is operating without the User "Opexec" started, the Validation Suite shall be invoked from the front panel keypad, either as a execution in a continuous loop or by individual test selections.

9.2.7.5.4
The validation suite shall execute as a task of the OS-9 Shell Utilities and Commands module. Execution from the shell shall be by typing "Valsuite" from the prompt. If the User Program has been executed, the VALSUITE shall not execute any of its tests due to resource conflicts. It shall be possible to execute the following additional CPU Module specific commands while in the OS-9 Shell Utility:

1. **Get/Set the hardware time of day clock**
2. **Set OS-9 clock from hardware clock**
3. **Read/write all I/O registers internal to the MC 68360**
4. **Get/Set all programmable controls on serial ports**
5. **Verify that the 120 Hz interrupt is functioning**
6. **Set, configure, and read timers**
7. **Observe time-out interrupts**

9.2.7.5.5
The OS-9 Shell Utility shall communicate with the user through the SP4 Port. When invoked, a low-priority task shall be executed for each SP port 1 and 2. Each task shall be configurable to use a different combination of input buffering options. The task shall open the port, configure it, and then enter a processing loop. In the loop, it shall wait for input and echo any input to the output. If no input is received for one second, an ASCII text string shall be sent out on the port. This text string shall be of the form *"port P hh:mm:ss."* P is the port number and hh:mm:ss is the current OS-9 time stamp. The text shall be terminated with a carriage return followed by a line feed character.

9.2.7.5.6*
Source and object Software shall be provided to the QPL or Purchasing Agency on both document listing and CD Memory. It shall provide user descriptions of test logic and reports. The Agency shall possess non- exclusive rights to this program suite.

9.2.7.6 RE-FLASH UTILITY
A Utility Program shall be provided that would allow the user to up-grade (re-flash) the Boot Image as defined in section 9.2.7. This utility shall provide the capabilities for upgrading the Operating System and drivers when available by the manufacturer. The Utility Program to shall provide the capability for the user to dynamically upgrade the Boot Image via the command prompt.

9.2.7.7 DELIVERABLES

9.2.7.7.1
A software package resident on the FLASH Memory shall be provided, including the Embedded OS-9 kernels, platform drivers, and a validation suite.

9.2.7.7.2
All software shall be delivered in the following forms:

1. **Fully commented source code of contractor developed software (OS-9 not required)**
2. **Microware Ultra-C Version 1.1 compatible linkable object code**
3. **Memory map listing**

9.2.7.7.3
Specific hardware memory addresses shall be specified and provided in a supplied INCLUDE FILE as defined constants. The INCLUDE FILE shall meet all applicable software delivery requirements.

9.2.7.7.4
Timer usage by drivers and their uninterrupted execution latencies, error values returned by driver calls, error codes, and a format of the error report file shall be documented.

9.2.7.7.5
Software to initialize and perform a power-up self-test of the CPU Module prior to the initialization of the OS-9 operating system shall be provided. All software components detailed in this specification or otherwise, and requiring initialization, shall be identified and the required initialization and nature of the test, documented. In addition, software provided to perform initialization and/or test shall be documented.

9.2.7.7.6
OS-9 compliant header files shall be provided with all Driver Modules.

CHAPTER 9 SECTION 3

MODEL 2070-2 FIELD I/O MODULE (FI/O)

9.3.1
The MODEL 2070-2A MODULE shall consist of the Field Controller Unit; Parallel Input/Output Ports; other Module Circuit Functions (includes muzzle jumper); Serial Communication Circuitry; Module Connectors C1S, C11S, and C12S mounted on the module front plate; VDC Power Supply (+12VDC to +5VDC); and required software.

9.3.2
The MODEL 2070-2B MODULE shall consist of the Serial Communication Circuitry, DC Power Supply, and Module Connector C12S mounted on the module front plate only.

9.3.3 FIELD CONTROLLER UNIT (FCU)

The FCU shall include a programmable microprocessor/controller unit together with all required clocking and support circuitry. Operational software necessary to meet housekeeping and functional requirements shall be provided resident in socketed firmware.

9.3.4 PARALLEL I/O PORTS

The I/O Ports shall provide 64 bits of input using ground-true logic. Each input shall be read logic "1" when the input voltage at its field connector input is less than 3.5 VDC, and shall be read logic "0" when either the input current is less than 100 µA or the input voltage exceeds 8.5 VDC. Each input shall have an internal pull-up to the isolated +12 VDC and shall not deliver greater than 20 mA to a short circuit to ground.

9.3.4.1
The I/O Ports shall provide 64 bits of output. Each output written as a logic "1" shall have a voltage at its field connector output of less than 4.0 VDC. Each output written as a logic "0" shall provide an open circuit (1 megohm or more) at its field connector output. Each output shall consist of an open-collector capable of driving 40 VDC minimum and sinking 100 mA minimum. Each output circuit shall be capable of switching from logic "1" to logic "0" within 100 µs when connected to a load of 100 K-Ohms minimum. Each output circuit shall be protected from transients of 10 ±2 µs duration, ±300 VDC from a 1 K-Ohm source, with a maximum rate of 1 pulse per second.

9.3.4.2
Each output shall latch the data written and remain stable until either new data is written or the active-low reset signal. Upon an active-low reset signal, each output shall latch a logic "0" and retain that state until a new writing. The state of all output circuits at the time of Power Up or in Power Down state shall be open. It shall be possible to simultaneously assert all outputs within 100 µs of each other. An output circuit state not changed during a new writing shall not glitch when other output circuits are updated.

9.3.5 OTHER MODULE CIRCUIT FUNCTIONS

9.3.5.1
A maximum capacitive load of 100 pF shall be presented to the LINESYNC input signal. The EIA-485 compliant differential LINESYNC signals shall be derived from the LINESYNC signal.

9.3.5.2
An External WDT "Muzzle" Jumper shall be provided on the board. With the jumper IN and NRESET transitions HIGH (FCU active), the FCU shall output a state change on Output Port 5, bit 8 (Connector C1, pin 103 - Monitor Watchdog Timer Input) every 100 ms for 3.5 seconds or due to CPU Command. When the jumper is missing, the feature shall not apply. This feature is required to operate with the Model 210 Monitor Unit only.

9.3.5.3
A WATCHDOG Circuit shall be provided. It shall be enabled by the FIELD I/O software at Power Up with a value of 100 ms. Its enabled state shall be machine readable and reported in the FI/O status byte. Once enabled, the watchdog timer shall not be disabled without resetting the FI/O. Failure of the FI/O to reset the watchdog timer within the prescribed timeout shall result in a hardware reset.

9.3.5.4 ONE KHz REFERENCE
A synchronizable 1 KHz time reference shall be provided. It shall maintain a frequency accuracy of ±0.01% (±0.1 counts per second).

9.3.5.5
A 32-bit MILLISECOND COUNTER (MC) shall be provided for "time stamping." Each 1 KHz reference interrupt shall increment the MC.

9.3.5.6
At Power Up, the FCU loss of communications timer shall indicate loss of communications until the user program sends the Request Module Status message to reset the "E" Bit and a subsequent set output command is processed.

9.3.5.7
A LOGIC Switch shall be provided resident on the module board. The switch shall function to disconnect Serial Port 3 (SP3) from the external world, Connector C12S. Its purpose is to prevent multiple use of SP3. An LED shall be provided on the module front panel labeled "SP3 ON". If LED lite ON, SP3 is active and available at C12S.

9.3.6* SERIAL COMMUNICATIONS / LOGIC CIRCUITRY

9.3.6.1*
System Serial Port 5 (SP5) EIA 485 signal Lines shall enter the I/O Module and be split into two multi-drop isolated ports. One shall be routed to the FCU and the other converted to EIA 485, then routed to Connector C12S.

9.3.6.2*
System Serial Port 3 (SP3) EIA 485 signal lines shall enter the I/O module and be isolated, converted back to EIA 485 and then routed to Connector C12S.

9.3.6.3*
LINESYNC and POWER DOWN Lines shall be split and isolated, one routed to FCU for shut down functions and the other changed to EIA 485; then routed to connector 12S for external module use.

9.3.6.4*
CPU RESET and POWER UP (SYSRESET) Lines shall be isolated and "OR'd" to form NRESET. NRESET shall be used to reset FCU and other module devices. NRESET shall also, be converted to EIA 485, then routed to Connector C12S.

9.3.6.5*
If the module is 2070-2B, routing to FCU does't apply.

9.3.6.6*
Isolation is between internal +5DC / DCG#1 and +12 DC ISO/DCG#2. +12 DC ISO shall be used for board power and external logic.

9.3.7 BUFFERS

A Transition Buffer shall be provided capable of holding a minimum of 1024 recorded entries. The Transition Buffer shall default to empty. There shall be two entry types: Transition and Rollover. The inputs shall be monitored for state transition. At each transition (If the input has been configured to report transition), a transition entry shall be added to the Transition Buffer. The MC shall be monitored for rollover. At each rollover transition ($xxxx FFFF - $xxxx 0000), a rollover entry shall be added to the Transition Buffer. For rollover entries, all bits of byte 1 are set to indicate that this is a rollover entry. Transition Buffer blocks are sent to the CPU module upon command. Upon confirmation of their reception, the blocks shall be removed from the Transition Buffer. The entry types are depicted as follows:

Input Transition Entry

Description	msb							lsb	Byte Number
Transition Entry Identifier	S	Input Number							1
Timestamp NLSB	x	x	x	x	x	X	x	x	2
Timestamp LSB	x	x	x	x	x	x	x	x	3

Millisecond Counter Rollover Entry

Description	msb							lsb	Byte Number
Rollover Entry Identifier	1	1	1	1	1	1	1	1	1
Timestamp MSB	x	x	x	x	x	x	x	x	2
Timestamp NMSB	x	x	x	x	x	x	x	x	3

9.3.8 I/O FUNCTIONS

9.3.8.1 INPUTS

Input scanning shall begin at I0 (bit 0) and proceed to the highest input, ascending from lsb to msb. Each complete input scan shall finish within 100 μs. Once sampled, the Logic State of input shall be held until the next input scan. Each input shall be sampled 1,000 times per second. The time interval between samples shall be 1 ms ±100 μs. If configured to report, each input that has transitioned since its last sampling shall be identified by input number, transition state, and timestamp (at the time the input scan began) and shall be added as an entry to the Transition Buffer. If multiple inputs change state during one input sample, these transitions shall be entered into the Input Transition Buffer by increasing number. The MC shall be sampled within 10 μs of the completion of the input scan.

9.3.8.2 DATA FILTERING

If configured, the inputs shall be filtered by the FCU to remove signal bounce. The filtered input signals shall then be monitored for changes as noted. The filtering parameters for each input shall consist of Ignore Input Flag and the On and Off filter samples. If the Ignore Input flag is set, no input transitions shall be recorded. The On and Off filter samples shall determine the number of consecutive samples an input must be on and off, respectively, before a change of state is recognized. If the change of state is shorter than the specified value, the change of state shall be ignored. The On and Off filter values shall be in the range of 0 to 255. A filter value of 0, for either or both values, shall result in no filtering for this input. The default values for input signals after reset shall be as follows:

Filtering	**Enabled**
On and off filter values shall be set to	**5**
Transition monitoring	**Disabled (Timestamps are not logged)**

9.3.8.3 OUTPUTS

Simultaneous assertion of all outputs shall occur within 100 μs. Each output shall be capable of being individually configured in state to ON, OFF, or a state synchronized with either phase of LINESYNC. The condition of the outputs shall only be "ON" if the FI/O continues to receive active communications from the CPU Module. If there is no valid communications with the CPU Module for 2.0 seconds, all outputs shall revert to the OFF

condition, and the FI/O status byte shall be updated to reflect the loss of communication from the CPU Module.

9.3.8.4 Standard Function

Each output shall be controlled by the data and control bits in the CPU Module Field I/O frame protocol as follows:

Output Bit Translation

Case	Output Data Bit	Output Control Bit	Function
A	0	0	Output in the OFF state
B	1	1	Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is OFF, and when LINESYNC is OFF (0), the output is ON.
C	0	1	Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is ON, and when LINESYNC is OFF (0), the output is OFF
D	1	0	Output is in the ON state.

9.3.8.4.1

In Case A above, the corresponding output shall be turned OFF if previously ON and if previously OFF remain OFF until otherwise configured. For half-cycle switching (cases B and C), all outputs to be changed shall be changed within 50 μs after the corresponding LINESYNC transition and shall remain in the same state during the entire half cycle. In Case D above, the corresponding output shall be turned ON if previously OFF and if previously ON remain ON until otherwise configured. All outputs shall not glitch nor change state unless configured to do so.

9.3.8.5 Interrupts

All interrupts shall be capable of asynchronous operation with respect to all processing and all other interrupts. MILLISECOND Interrupt shall be activated by the 1 KHz reference once per ms. A timestamp rollover flag set by MC rollover shall be cleared only on command. LINESYNC Interrupt - This interrupt shall be generated by both the 0-1 and 1-0 transitions of the LINESYNC signal. The LINESYNC interrupt shall monitor the MC interrupt and set the MC error flag if there has not been an interrupt from the 1 KHz source for 0.5 seconds ($\geq$60 consecutive LINESYNC interrupts). The LINESYNC interrupt shall synchronize the 1 KHz time reference with the 0-1 transition of the LINESYNC signal once a second. A LINESYNC error flag shall be set if the LINESYNC interrupt has not successfully executed for 0.5 seconds or longer ($\geq$500 consecutive millisecond interrupts).

9.3.8.6 Communication Service Routine

A low-level communication service routine shall be provided to handle reception, transmission, and EIA-485 communication faults. The communication server shall automatically:

For Transmission:

Generate the opening and closing flags
Generate the CRC value
Generate the abort sequence (minimum of 8 consecutive '1' bits) when commanded by the FCU
Provide zero bit insertion

For Receiving:

Detect the opening and closing flags
Provide address comparison, generating an interrupt for messages addressed to the I/O Module, and ignoring messages not addressed to the I/O Module
Strip out inserted zeros
Calculate the CRC value, compare it to the received value, and generate an interrupt on an error
Generate an interrupt if an abort sequence is received

9.3.8.7 Communication Processing

The task shall be to process the command messages received from the CPU Module, prepare, and start response transmission. The response message transmission shall begin within 4 ms of the receipt of the received message. Message type processing time constraints shall not exceed 70 ms per message.

9.3.8.8 Input Processing

This task shall process the raw input data scanned in by the 1 ms interrupt routine, perform all filtering, and maintain the transition queue entries.

9.3.9
DATA COMMUNICATION PROTOCOLS

9.3.9.1

Protocols - All communication with the CPU Module shall be SDLC-compatible command-response protocol, support 0 bit stuffing, and operate at a data rate of 614.4 Kbps. The CPU Module shall always initiate the communication and should the command frame be incomplete or in error, no FI/O response shall be transmitted. The amount of bytes of a command or response is dependent upon the I/O Module identification.

9.3.9.1.1

The frame type shall be determined by the value of the first byte of the message. The command frames type values $70 - $7F and associated response frame type values $F0 - $FF are allocated to the Contractor diagnostics. All other frame types not called out are reserved. The command-response Frame Type values and message times shall be as follows:

Frame Types

Module Command	I/0 Module Response	Description	Minimum Message Time	Maximum Message Time
49	177	Request Module Status	250 μs	275 us
50	178	MILLISECOND CTR. Mgmt.	222.5 μs	237.5 us
51	179	Configure Inputs	344.5 μs	6.8750 ms
52	180	Poll Raw Input Data	317.5 μs	320 μs
53	181	Poll Filtered Input Data	317.5 μs	320 μs
54	182	Poll Input Transition Buffer	300 μs	10.25 ms
55	183	Command Outputs	405 μs	410 μs
56	184	Config. Input Tracking Functions	340 μs	10.25 ms
57	185	Config. Complex Output Functions	340 μs	6.875 ms
58	186	Configure Watchdog	222.5 μs	222.5 μs
59	187	Controller Identification	222.5 μs	222.5 μs
60	188	I/O Module Identification	222.5 μs	222.5 μs
61-62-65 63 64	189-190-193 191 192	Reserved (note below) Poll variable length raw input Variable length command outputs	 317.5 us 405 us	 320 us 410 us

9.3.9.1.2

Messages 61/189, and 62/190, and 65/193 are for ITS Cabinet Monitor Unit. See ITS Cabinet Monitor System Serial Bus #1 for Command and Response Frames (See Chapter 3). Message 63 / Message 191 shall be the same as Message 52/180 except Byte 2 of Message 180 response shall denote the following number of inputs bytes. Message 64/192 shall be the same as Message 55/183 except Byte 2 of the Message 55 Command shall denote the number of output data bytes along with the following output data.

9.3.9.2 REQUEST MODULE STATUS

The Command shall be used to request FI/O status information response.
Command/response frames are as follows:

Request Module Status Command

Description	Msb							lsb	Byte Number
(Type Number = 49)	0	0	1	1	0	0	0	1	Byte 1
Reset Status Bits	P	E	K	R	T	M	L	W	Byte 2

Request Module Status Response

Description	Msb							lsb	Byte Number
(Type Number = 177)	1	0	1	1	0	0	0	1	Byte 1
System Status	P	E	K	R	T	M	L	W	Byte 2
SCC Receive Error Count	Receive Error Count								Byte 3
SCC Transmit Error Count	Transmit Error Count								Byte 4
Timestamp MSB	Timestamp MSB								Byte 5
Timestamp NMSB	Timestamp NMSB								Byte 6
Timestamp NLSB	Timestamp NLSB								Byte 7
Timestamp LSB	Timestamp LSB								Byte 8

9.3.9.2.1
The response status bits are defined as follows:

P - Indicates FI/O hardware reset
E - Indicates a communications loss of greater than 2 seconds
M - Indicates an error with the MC interrupt
L - Indicates an error in the LINESYNC
W - Indicates that the FI/O has been reset by the Watchdog
R - Indicates that the EIA-485 receive error count byte has rolled over
T - Indicates that the EIA-485 transmit error count byte has rolled over
K - Indicates the Datakey has failed or is not present

9.3.9.2.2
Each of these bits shall be individually reset by a '1' in the corresponding bit of any subsequent Request Module Status frame, and the response frame shall report the current status bits. The SCC error count bytes shall not be reset. When a count rolls over (255 - 0), its corresponding roll-over flag shall be set.

9.3.9.3
MC MANAGEMENT frame shall be used to set the value of the MC. The 'S' bit shall return status '0' on completion or '1' on error. The 32-bit value shall be loaded into the MC at the next 0-1 transition of the LINESYNC signal. The frames are as follows:

Millisecond Counter Management Command

Description	msb							Lsb	Byte Number
(Type Number = 50)	0	0	1	1	0	0	1	0	Byte 1
New Timestamp MSB	x	X	x	X	x	x	x	x	Byte 2
New Timestamp NMSB	x	X	x	X	x	x	x	x	Byte 3
New Timestamp NLSB	x	X	x	X	x	x	x	x	Byte 4
New Timestamp LSB	x	X	x	X	x	x	x	x	Byte 5

Millisecond Counter Management Response

Description	msb							Lsb	Byte Number
(Type Number = 178)	1	0	1	1	0	0	1	0	Byte 1
Status	0	0	0	0	0	0	0	S	Byte 2

9.3.9.4 CONFIGURE INPUTS

The Configure Inputs command frame shall be used to change input configurations. The command-response frames are as follows:

Configure Inputs Command

Description	msb							Lsb	Byte Number
(Type Number = 51)	0	0	1	1	0	0	1	1	Byte 1
Number of Items (n)	n	N	n	N	n	n	n	n	Byte 2
Item # - Byte 1	E	Input Number							Byte 3(I-1)+3
Item # - Byte 2	Leading edge filter (e)								Byte 3(I-1)+4
Item # - Byte 3	Trailing edge filter (r)								Byte 3(I-1)+5

Configure Inputs Response

Description	msb							Lsb	Byte Number
(Type Number = 179)	1	0	1	1	0	0	1	1	Byte 1
Status	0	0	0	0	0	0	0	S	Byte 2

Block field definitions shall be as follows:

E - Ignore Input Flag. "1" = do not report transitions for this input, "0" = report transitions for this input

e - A one-byte leading edge filter specifying the number of consecutive input samples which must be "0" before the input is considered to have entered to "0" state from "1" state (range 1 to 255, 0 = disabled)

r - A one-byte trailing edge filter specifying the number of consecutive input samples which must be "1" before the input is considered to have entered to "1" state from "0" state (range 1 to 255, 0 = disabled)

S - return status S = '0' on completion or '1' on error

9.3.9.5 POLL RAW INPUT DATA

The Poll Raw Input Data frame shall be used to poll the FI/O for the current unfiltered status of all inputs. The response frame shall contain 8 or 15 bytes of information indicating the current input status. The frames are as follows:

Poll Raw Input Data Command

Description	Msb							lsb	Byte Number
(Type Number = 52)	0	0	1	1	0	1	0	0	Byte 1

Poll Raw Input Data Response

Description	msb							lsb	Byte Number
(Type Number = 180)	1	0	1	1	0	1	0	0	Byte 1
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x	Byte 2
Inputs I8 to I119	x	x	x	x	x	x	x	x	Bytes 3 to 16
Timestamp MSB	x	x	x	x	x	x	x	x	Byte 17
Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 18
Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 19
Timestamp LSB	x	x	x	x	x	x	x	x	Byte 20

9.3.9.6 POLL FILTERED INPUT DATA

The Poll Filtered Input Data frame shall be used to poll the FI/O for the current filtered status of all inputs. The response frame shall contain 8 bytes (2A) or 15 bytes (2B) of information indicating the current filtered status of the inputs. Raw input data shall be provided in the response for inputs that are not configured for filtering. The frames are as follows:

Poll Filter Input Data Command

Description	Msb							lsb	Byte Number
(Type Number = 53)	0	0	1	1	0	1	0	1	Byte 1

Poll Filter Input Data Response

Description	msb							lsb	Byte Number
(Type Number = 181)	1	0	1	1	0	1	0	1	Byte 1
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x	Byte 2
Inputs I8 to I119	x	x	x	x	x	x	x	x	Bytes 3 to 16
Timestamp MSB	x	x	x	x	x	x	x	x	Byte 17
Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 18
Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 19
Timestamp LSB	x	x	x	x	x	x	x	x	Byte 20

9.3.9.7 POLL INPUT TRANSITION BUFFER

The Poll Input Transition Buffer frame shall poll the FI/O for the contents of the input transition buffer. The response frame shall include a three-byte information field for each of the input changes that have occurred since the last interrogation. The frames are as follows:

Poll Input Transition Buffer Command

Description	msb							lsb	Byte Number
(Type Number = 54)	0	0	1	1	0	1	1	0	Byte 1
Block Number	x	x	x	X	x	X	x	x	Byte 2

Input Transition Buffer Response

Description	msb							lsb	Byte Number
(Type Number = 182)	1	0	1	1	0	1	1	0	Byte 1
Block Number	x	x	x	X	x	X	x	x	Byte 2
Number of Entries	x	x	x	X	x	X	x	x	Byte 3
Item #	S	Input Number							Byte 3(I-1)+4
Item # Timestamp NLSB	x	x	x	X	x	X	x	x	Byte 3(I-1)+5
Item # Timestamp LSB	x	x	x	X	x	X	x	x	Byte 3(I-1)+6
Status	0	0	0	0	C	F	E	G	Byte 3(I-1)+7
Timestamp MSB	x	x	x	X	x	X	x	X	Byte 3(I-1)+8
Timestamp NMSB	x	x	x	X	x	X	x	X	Byte 3(I-1)+9
Timestamp NLSB	x	x	x	X	x	X	x	X	Byte 3(I-1)+10
Timestamp LSB	x	x	x	X	x	X	x	X	Byte 3(I-1)+11

9.3.9.7.1
Each detected state transition for each active input (see configuration data) is placed in the queue as it occurs. Bit definitions are as follows:

- **S Indicates the state of the input after the transition**
- **C Indicates the 255 entry buffer limit has been exceeded**
- **F Indicates the 1024 buffer limit has been exceeded**
- **G Indicates the requested block number is out of monotonic increment sequence**
- **E Same block number requested, E is set in response**

9.3.9.7.2
The Block Number byte is a monotonically increasing number incremented after each command issued by the CPU Module. When the FI/O Module receives this command, it shall compare the associated Block Number with the Block Number of the previously received command. If it is the same, the previous buffer shall be re-sent to the CPU Module and the 'E' flag set in the status response frame. If it is not equal to the previous Block Number, the old buffer shall be purged and the next block of data sent. If the block number is not incremented by one, the status G bit shall be set. The block number received

becomes the current number (even if out of sequence). The Block Number byte sent in the response block shall be the same as that received in the command block. Counter rollover shall be considered as a normal increment.

9.3.9.8 SET OUTPUTS

The Set Outputs frame shall be used to command the FI/O to set the Outputs according to the data in the frame. If there is any error configuring the outputs, the 'E' flag in the response frame shall be set to '1'. If the LINESYNC reference has been lost, the 'L' bit in the response frame shall be set. Loss of LINESYNC reference shall also be indicated in system status information. The output bytes depend upon field I/O module. These command and response frames are as follows:

Set Outputs Command

Description	Msb							lsb	Byte Number
(Type Number = 55)	0	0	1	1	0	1	1	1	Byte 1
Outputs O0 (lsb) to O7 (msb) Data	X	x	x	X	x	X	x	x	Byte 2
Outputs O8 to O103 Data	X	x	x	X	x	X	x	x	Bytes 3 to 14
Outputs O0 (lsb) to O7 (msb) Control	X	x	x	X	x	X	x	x	Byte 15
Outputs O8 to O103 Control	X	x	x	X	x	X	x	x	Bytes 16 to 27

Set Outputs Response

Description	Msb							lsb	Byte Number
(Type Number = 183)	1	0	1	1	0	1	1	1	Byte 1
Status	0	0	0	0	0	0	L	E	Byte 2

9.3.9.9 CONFIGURE INPUT TRACKING FUNCTIONS

The Configure Input Tracking Functions frame shall be used to configure outputs to respond to transitions on a specified input. Each Output Number identified by Item Number shall respond as configured to the corresponding Input Number identified by the same Item Number. Input to Output mapping shall be one to one. If a command results in more than 8 input tracking outputs being configured, the response V bit shall be set to '1' and the command shall not be implemented. The command and response frames are as follows:

Configure Input Tracking Functions Command

Description	msb							lsb	Byte Number
(Type Number = 56)	0	0	1	1	1	0	0	0	Byte 1
Number of Items	Number of Items								Byte 2
Item # - Byte 1	E	Output Number							Byte 2(I-1)+3
Item # - Byte 2	I	Input Number							Byte 2(I-1)+4

Configure Input Tracking Functions Response

Description	msb							lsb	Byte Number
(Type Number = 184)	1	0	1	1	1	0	0	0	Byte 1

Status	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**V**	**Byte 2**
Timestamp MSB	**x**	**x**	**x**	**X**	**x**	**x**	**x**	**x**	**Byte 3**
Timestamp NMSB	**x**	**x**	**x**	**X**	**x**	**x**	**x**	**x**	**Byte 4**
Timestamp NLSB	**x**	**x**	**x**	**X**	**x**	**x**	**x**	**x**	**Byte 5**
Timestamp LSB	**x**	**x**	**x**	**X**	**x**	**x**	**x**	**x**	**Byte 6**

9.3.9.9.1
Definitions are as follows:

E '1' - Enable input tracking functions for this output
'0' - Disable input tracking functions for this output
I '1' - The output is OFF when input is ON, ON when input OFF
'0' - The output is ON when input is ON, OFF when input is OFF
V '1' - The max. number of 8 configurable outputs has been exceeded
'0' - No error

Number of Items - The number of entries in the frame. If zero, all outputs currently configured for input tracking shall be disabled.

9.3.9.9.2
The timestamp value shall be sampled prior to the response frame.

9.3.9.9.3
Outputs which track inputs shall be updated no less than once per ms. Input to output signal propagation delay shall not exceed 2 ms.

9.3.9.9.4
The "Number of Item" field is valid from 0 to 16 (most that is sent at one time is 8 enables and 8 disables). If processing a command resulting in more than 8 Input Tracking functions being enabled, none of the command shall be implemented and response message "V" bit set to 1. If an invalid output or input number is specified for a function, the FIOM software shall not do that function definition. It shall also not be counted toward the maximum of 8 input tracking function allowed. The rest of the message shall be processed. When an Input Tracking function is disabled, the output is set according to the most recently received Set Outputs Command. When an input tracking function for an output is superseded (redefined as either another input tracking function, or as a complex output function) nothing shall be done with the output. The most recent value remains until the new function changes it.

9.3.9.10
CONFIGURE COMPLEX OUTPUT FUNCTIONS - The Configure Complex Output Functions frame shall be used to specify a complex output for one to eight of any of the outputs. If a Configure Complex Output Function command results in more than eight outputs being configured, the 'V' bit in the response message shall be set to a '1', and the command shall not be implemented. Two output forms shall be provided, single pulse and continuous oscillation. These output forms shall be configurable to begin immediately or on

a specified input trigger and, in the case of continuous oscillation, to continue until otherwise configured or to oscillate only while gated active by a specified input. If the command gate bit is active, the command trigger bit shall be ignored and the specified input shall be used as a gate signal. The command and response frames are as follows:

Configure Complex Output Functions Command

Description	msb							lsb	Byte Number
(Type Number = 57)	0	0	1	1	1	0	0	1	Byte 1
Number of Items	Number of Items								Byte 2
Item # - Byte 1	0	Output Number							Byte 7(I-1)+3
Item # - Byte 2	Primary Duration (MSB)								Byte 7(I-1)+4
Item # - Byte 3	Primary Duration (LSB)								Byte 7(I-1)+5
Item # - Byte 4	Secondary Duration (MSB)								Byte 7(I-1)+6
Item # - Byte 5	Secondary Duration (LSB)								Byte 7(I-1)+7
Item # - Byte 6	0	Input Number							Byte 7(I-1)+8
Item # - Byte 7	P	W	G	E	J	F	R	L	Byte 7(I-1)+9

Configure Complex Output Functions Response

Description	msb							lsb	Byte Number
(Type Number = 185)	1	0	1	1	1	0	0	1	Byte 1
Status	0	0	0	0	0	0	0	V	Byte 2
Timestamp (MSB)	x	x	x	X	x	x	x	x	Byte 3
Timestamp (NMSB)	x	x	x	X	X	x	x	x	Byte 4
Timestamp (NLSB)	x	X	x	X	X	x	x	x	Byte 5
Timestamp (LSB)	x	X	x	X	X	x	x	x	Byte 6

9.3.9.10.1
The bit fields of the command frame are defined as follows:

E '1' - enable complex output function for this output
'0' - disable complex output function for this output

J '1' - During the primary duration, the output shall be written as a logic '1'. During the secondary duration, the output shall be written as a logic '0'.
'0' - During the primary duration, the output shall be written as a logic '0'. During the secondary duration, the output shall be written as a logic '1'.

Output Number - 7-bit output number identifying outputs
Primary Duration - For single pulse operation, this shall determine the number of 'ticks' preceding the pulse. For continuous oscillation, this shall determine the length of the inactive (first) portion of the cycle.

Secondary Duration - For single pulse operation, this shall determine the number of 'ticks' the pulse is active. Subsequent to the secondary duration, the output shall return to the state set according to the most recently received Set Outputs command. For continuous oscillation, this shall determine the length of the active (second) portion of the cycle. 0 = hold output state until otherwise configured.

F '1' - The trigger or gate shall be acquired subsequent to filtering the specified input. The raw input signal shall be used if filtering is not enabled for the specified input.

'0' - The trigger or gate shall be derived from the raw input.

R '1' - For triggered output, the output shall be triggered by an ON-to-OFF transition of the specified input and shall be triggered immediately upon command receipt if the input is OFF. For gated output, the output shall be active while the input is OFF.

'0' - For triggered output, the output shall be triggered by an OFF-to-ON transition of the specified input and shall be triggered immediately upon command receipt if the input is ON. For gated output, the output shall be active while the input is ON.

Input Number - 7-bit input number identifying inputs 0 Up.

P '1' - The output is configured for single-pulse operation. Once complete, the complex output function shall be disabled.

'0' - The output is configured for continuous oscillation.

W '1' - It is triggered by the specified input. Triggered complex output shall commence within 2 ms of the associated trigger.

'0' - Operation shall begin within 2 ms of the command receipt.

G '1' - Operation shall be gated active by the specified input.

'0' - Gating is inactive.

L '1' - The LINESYNC based clock shall be used for the time ticks.

'0' - The MC shall be used for the time ticks.

V '1' - Indicates maximum number of configurable outputs is exceeded.

'0' - No error

Number of items - The number of entries in the frame. If 0, all outputs currently configured as complex outputs shall be disabled.

9.3.9.10.2
Controlling input signals shall be sampled at least once per millisecond.

9.3.9.10.3
The "Number of Items" field is valid from 0 to 16. Zero means disable all Complex Output functions. Sixteen is the maximum because the most that is sent at one time is 8 enables and 8 disables. If processing a command results in more than 8 Complex Output functions being enabled, none of the command shall be implemented and the response message "V" bit shall be set to 1. If an invalid output or input number (the "G" or "W" bits being set to 1 is specified for a function, that function definition is not done by the FIOM software. It

shall also not be counted towards the maximum of 8 Complex Output functions allowed. The rest of the message shall be processed. When a Complex Output function is disabled, the output is set according to the most recently received Set Outputs command. When a complex output function for an output is superseded, that is, redefined as wither another Complex Output function, or as an Input Tracking function, nothing special is done with the output. The most recent value remains until the new function changes it. The "G" bit (gating) set to 1 takes precedence over the "W" bit (triggering). If gating is ON, triggering is turned OFF, regardless of the value of the "W" bit in the command message. If a Complex Output is configured with the "G" bit set to 1 (gating) and the "P" bit set to 0 (continuous oscillation), the output is set to OFF (0) whenever the specified input changes state so that the oscillation should cease (output inactive). For a single pulse operation ("G" bit set to 1), after the secondary duration completes the Complex Output function shall be disabled, and the output shall be set according to the most recently received Set Outputs command.

9.3.9.11 CONFIGURE WATCHDOG

The Configure Watchdog frames shall be used to change the software watchdog timeout value. The Command and response frames are as follows:

Configure Watchdog Command

Description	msb							lsb	Byte Number
(Type Number = 58)	0	0	1	1	1	0	1	0	Byte 1
Timeout Value	x	x	x	X	x	x	x	x	Byte 2

Configure Watchdog Response

Description	msb							lsb	Byte Number
(Type Number = 186)	1	0	1	1	1	0	1	0	Byte 1
Status	0	0	0	0	0	0	0	Y	Byte 2

9.3.9.11.1

The timeout value shall be in the range between 10 to 100 ms. If the value is lower than 10, 10 shall be assumed. If the value is greater than 100, 100 shall be assumed.

9.3.9.11.2

On receipt of this frame, the watchdog timeout value shall be changed to the value in the message and the "Y" bit set. The response frame bit (Y) shall indicate a '1' if the watchdog has been previously set and a '0' if not.

9.3.9.12 CONTROLLER IDENTIFICATION

This is a legacy message command / response for FI/O modules with Datakey resident. Upon command, a response frame containing the 128 bytes of the Datakey. On NRESET transition to High or immediately prior to any interrogation of the Datakey, the FI/O shall test the presence of the Key. If absent, the FI/O Status Bit "K" shall be set and no interrogation shall take place. If an error occurs during the interrogation, Bit "K" shall be

set. If "K" bit set, only the first two bytes shall be returned. The Command Response frames are as follows:

Controller Identification Command

Description	msb							lsb	Byte Number
(Type Number = 59)	0	0	1	1	1	0	1	1	Byte 1

Controller Identication Response

Description	msb							lsb	Byte Number
(Type Number = 187)	1	0	1	1	1	0	1	1	Byte 1
Status	0	0	0	0	0	0	0	K	Byte 2
Datakey	x	x	x	x	x	x	x	x	Byte 3 to 130

9.3.9.13 MODULE IDENTIFICATION

The FI/O Identification command frame shall be used to request the FI/O Identification value Response of 20 for the 2070-2A or 2070-8 FI/O, and the frame address. The address for ITS Cabinet SIUs and CMU shall be frame address (See Chapter 3). The command and response frames are shown as follows:

I/O Module Identification Command

Description	msb							lsb	Byte Number
(Type Number = 60)	0	0	1	1	1	1	0	0	Byte 1

I/O Module Identification Response

Description	msb							lsb	Byte Number
(Type Number = 188)	1	0	1	1	1	1	0	0	Byte 1
FI/O ID byte	x	x	x	X	x	x	x	x	Byte 2

CHAPTER 9 SECTION 4

MODEL 2070-3 FRONT PANEL ASSEMBLY (FPA)

9.4.1
The Model 2070-3 Front Panel Assembly shall be delivered with one of the three options as called out under Chapter 9, Section 1 or in the contract's special provisions (governs). All options shall consist of a panel with latch assembly and two TSD #1 hinge attaching devices, assembly PCB, external serial port connector(s), CPU active LED indicator, and FP Harness Interface. The options shall include the additional features, as follows:

OPTION 3A - FPA controller, two keyboards, AUX switch, alarm bell & Display A
OPTION 3B - FPA controller, two keyboards, AUX switch, alarm bell & Display B
OPTION 3C - System Serial Port 6 Lines, isolated and vectored to Connector C60S.

9.4.2
Two KEYBOARDS shall be provided, one with sixteen keys for hexadecimal alphanumeric entry and the other with twelve keys to be used for cursor control and action symbol entry. Each key shall be engraved or embossed with its function character. Each key shall have an actuation force between 50 and 100 grams and provide a positive tactile indication of contact closure. Key contacts shall be hermetically sealed, have a design life of over one million operations, shall be rated for the current and voltage levels used, and shall stabilize within 5 ms following contact closure.

9.4.3
The cathode of the CPU ACTIVE LED INDICATOR shall be electrically connected to the CPU Activity LED signal and shall be pulled up to +5 VDC.

9.4.4
The DISPLAY shall consist of a Liquid Crystal Display (LCD), a backlight, and a contrast potentiometer control. Display A shall have 4 lines of 40 characters each with a minimum character dimensions of 5.00 mm wide by 10.44 mm high and an electro-luminescent (EL) backlight. Display B shall have 8 lines of 40 characters each with minimum dimensions of 2.65 mm wide by 4.24 mm high and either LED or EL backlight.

9.4.4.1
Each character shall be composed of a 5x7 dot matrix with a underline row or a 5x8 dot matrix. The viewing angle of the LCD shall be optimized for direct (90^{o}) viewing, $\pm 35^{o}$ vertical, $\pm 45^{o}$ horizontal. The LCD shall have variable contrast with a minimum ratio of 4:1. The LCD shall be capable of displaying, at any position on the Display, any of the standard ASCII characters as well as user-defined characters.

9.4.4.2
The backlight shall be turned on and off by the Controller Circuitry. The backlight and associated circuitry shall consume no power when in off state. A potentiometer shall control the LCD contrast with clockwise rotation increasing contrast. The contrast shall

depend on the angular position of the potentiometer, which shall provide the entire contrast range of the LCD.

9.4.4.3
Cursor display shall be turned ON and OFF by command. When ON, the cursor shall be displayed at the current cursor position. When OFF, no cursor shall be displayed. All other cursor functions (positioning, etc.) shall remain in effect.

9.4.5
The FPA CONTROLLER shall function as the Front Panel Device controller interfacing with the CPU Module.

9.4.5.1
A FPA RESET Switch shall be provided on the Assembly PCB. The momentary CONTROL switch shall be logic OR'd with the CPU RESET Line, producing a FPA RESET Output. Upon FPA RESET being active or receipt of a valid Soft Reset display command, the following shall occur:

1. **Auto-repeat, blinking, auto-wrap, and auto-scroll shall be set to OFF.**
2. **Each special character shall be set to ASCII SPC (space).**
3. **The tab stops shall be set to columns 9, 17, 25, and 33.**
4. **The backlight timeout value shall be set to 6 (60 seconds).**
5. **The backlight shall be extinguished.**
6. **The display shall be cleared (all ASCII SPC).**
7. **The FPA module shall transmit a power up string through /sp6 to the CPU once power is applied to the FPA, or the FPA hardware RESET BUTTON IS PUSHED. The string is " ESC CPU", hex value "1B 5B 50 C55".**

9.4.5.2
When a key press is detected, the appropriate key code shall be transmitted to SP6-RxD. If two or more keys are depressed simultaneously, no code shall be sent. If a key is depressed while another key is depressed, no additional code shall be sent.

9.4.5.3
Auto-repeat shall be turned ON and OFF by command. When ON, the key code shall be repeated at a rate of 5 times per second starting when the key has been depressed continuously for 0.5 second, and shall terminate when the key is released or another key is pressed.

9.4.5.4
When the AUX Switch is toggled, the appropriate AUX Switch code shall be transmitted to the CPU.

9.4.5.5
The controller circuitry shall be capable of composing and storing eight special graphical characters on command, and displaying any number of these characters in combination

with the standard ASCII characters. Undefined characters shall be ignored. User-composed characters shall be represented in the communication protocol on Page 9-7-12. P1 represents the special character number (1-8). Pn's represent columns of pixels from left to right. The most significant bit of each Pn represents the top pixel in a column and the least significant bit shall represent the bottom pixel. A logic '1' shall turn the pixel ON. There shall be a minimum of 5 Pn's for 5 columns of pixels in a command code sequence terminated by an "f." If the number of Pn's are more than the number of columns available on the LCD, the extra Pn's shall be ignored. P1 and all Pn's shall be in ASCII coded decimal characters without leading zero.

9.4.5.6
Character overwrite mode shall be the only display mode supported. A displayable character received shall always overwrite the current cursor position on the Display. The cursor shall automatically move right one character position on the Display after each character write operation. When the rightmost character on a line (position 40) has been overwritten, the cursor position shall be determined based on the current settings of the auto-wrap mode.

9.4.5.7
Auto-wrap shall be turned ON & OFF by command. When ON, a new line operation shall be performed after writing to position 40. When OFF, upon reaching position 40, input characters shall continue to overwrite position 40.

9.4.5.8
Cursor positioning shall be non-destructive. Cursor movement shall not affect the current display, other than blinking the cursor momentarily and periodically hiding the character at that cursor position.

9.4.5.9
Blinking characters shall be supported, and shall be turned ON and OFF by command. When ON, all subsequently received displayable characters shall blink at the rate of 1 Hz with a 60% ON / 40% OFF duty cycle. It shall be possible to display both blinking and non-blinking characters simultaneously.

9.4.5.10
Tab stops shall be configurable at all columns. A tab stop shall be set at the current cursor position when a SetTabStop command is received. Tab Stop(s) shall be cleared on receipt of a ClearTabStop command. On receipt of the HT (tab) code, the cursor shall move to the next tab stop to the right of the cursor position. If no tab stop is set to the right of the current cursor position, the cursor shall not move.

9.4.5.11
Auto-scroll shall be turned ON and OFF by command. When ON, a Line Feed or new line operation from the bottom line shall result in the display moving up one line. When OFF, a Line Feed or new line from the bottom line shall result in the top line clearing, and the cursor being positioned on the top line.

9.4.5.12
Displayable characters shall be refreshed at least 20 times per second.

9.4.5.13
The Display back light shall illuminate when any key is pressed and shall illuminate or extinguish by command. The backlight shall extinguish when no key is pressed for a specified time. This time shall be program selected by command, by a number in the range 0 to 63 corresponding to that number of 10-second intervals. A value of 1 shall correspond to a timeout interval of 10 seconds. A value of 0 shall indicate no timeout.

9.4.5.14
The Command Codes shall use the following conventions:

1. Parameters and Options: Parameters are depicted in both the ASCII and hexadecimal representations as the letter 'P' followed by a lower-case character or number. These are interpreted as follows:

- **Pn: Value parameter, to be replaced by a value, using one ASCII character per digit without leading zeros.**
- **P1: Ordered and numbered parameter. One of a listed known parameters with a specified order and number (Continues with P2, P3, etc.)**
- **Px: Display column number (1-40), using one ASCII character per digit without leading zero.**
- **Py: Display line (1-4) one ASCII character**
- **...: Continue the list in the same fashion**

Values of 'h' ($68) and 'l' ($6C) are used to indicate binary operations. 'h' represents ON (high), 'l' represents OFF (low).

2. ASCII Representation: Individual characters are separated by spaces; these are not to be interpreted as the space character, which is depicted by SPC.

3. Hexadecimal Representation: Characters are shown as their hexadecimal values and will be in the range 00 to 7F (7 bits).

9.4.5.15
The Controller Circuit shall communicate via a SP6 asynchronous serial interface. The interface shall be configured for 38.4 Kbps, 8 data bits, 1 stop bit, and no parity.

9.4.5.16*
C50 ENABLE function when grounded by Connector C50 Pins 1 and 5 shall be brought to Connector A1 Pin B21 for the purpose of disabling the module Channel 2.

9.4.6

The Front Panel shall include an electronic bell to signal receipt of ^G (hex 07). The bell shall sound at 2,000 Hz, with a minimum output rating of 85 dB upon receipt of ^G (hex 07). Receipt of all other characters and ESC codes shall continue during the time the bell sounds.

CHAPTER 9 SECTION 5

MODEL 2070-4 POWER SUPPLY MODULE

9.5.1
The Model 2070-4 Power Supply Module shall be independent, self contained Module, vented, and cooled by convection only. The Module shall slide into the unit's power supply compartment from the back of the Chassis and be attached to the Backplane Mounting Surface by its four TSD #3 Devices. The Model 2070-4B Module shall meet the same requirements as the 2070-4A except for 3.5 Amperes of +5 VDC.

9.5.2
An "On/Off" POWER Switch, four LED DC Power Indicators, PS Receptacle POWER Connectors, and the Incoming AC Fuse protection shall be provided on the Module Front. The LED DC POWER Indicators shall indicate all required DC voltages meet the following conditions: the +5 VDC is within 5% and the 12 VDC is within 8% of their nominal levels.

9.5.3
INPUT PROTECTION - Two 0.5-Ohm, 10-watt wire-wound power resistors with a 0.2 µH inductance shall be provided (one on the AC+ Line & on the AC- Line). Three 20 Joule surge arresters shall be provided between AC+ to AC-, AC+ to EG, and AC- to EG. A 0.68 µF capacitor shall be placed between AC+ & AC- (between the resistor & arresters).

9.5.4*
+5 VDC STANDBY POWER shall be provided to hold up specified circuitry during the power down period. It shall consist of the monitor circuitry, hold up capacitors, and charging circuitry. A charging circuit shall be provided, that under normal operation, shall fully charge and float the capacitors consistent with the manufacturers' recommendations. The Hold Up power requirements shall be a minimum constant drain of 600 µA at a range of +5 to +2 VDC for over 600 minutes.

9.5.5
MONITOR CIRCUITRY shall be provided to monitor incoming AC Power for Power Failure and Restoration and LINESYNC generation.

9.5.5.1
The AC FAIL/POWER DOWN Output Lines shall go LOW (ground true) immediately upon Power Failure. The Lines shall transition to HIGH at Power Restoration. The Lines shall be driven separately. The SYSRESET/POWERUP Output Lines shall transition to LOW 525 +/-25 ms after AC FAIL/POWER DOWN transition to LOW. The Lines shall transition to HIGH 225 +/- 25 ms after Power Restoration and the supply is fully recovered. The Lines shall be driven separately.

9.5.5.2
The monitor circuitry shall switch the +5 VDC Standby ON immediately upon Power Failure and isolate (OFF) the line at Power Up.

9.5.5.3 *

The 60 Hz Square Wave LINESYNC signal shall be generated by a crystal oscillator, which shall synchronize to the 60-Hz VAC incoming power line at 120 and 300 degrees. A continuous square wave signal shall be +5 VDC amplitude, 8.333 ms half-cycle pulse duration, and 50 ± 1% duty cycle. The output shall have drive sink capability of 16 mA. A 2 K-Ohm pull-up resistor shall be connected between the output and +5 VDC. The monitor circuit shall compensate for missing pulses and line noise during normal operation.

9.5.5.4

The LINESYNC shall continue until SYSRESET transitions LOW and begin then SYSRESET transitions HIGH.

9.5.6

POWER SUPPLY REQUIREMENTS

Voltage	Tolerances	I Minimum	I Maximum
+5 VDC	+4.875 to +5.125 VDC	1.0 AMP	10.0 AMP - MODULE 2070-4A 3.5 AMP – MODULE 2070-4B
+12 VDC Serial	+11.4 to +12.6 VDC	0.1 AMP	0.5 AMP
-12 VDC Serial	-11.4 to –12.6 VDC	0.1 AMP	0.5 AMP
+12 VDC	+11.4 to +12.6 VDC	0.1 AMP	1.0 AMP

9.5.6.1	Line / Load Regulation	-	shall meet the table tolerances values for voltage range of 90 to 135 VAC, minimum and maximum loads called out in the table & including ripple noise.
9.5.6.2	Efficiency	-	70 % minimum
9.5.6.3	Ripple & noise	-	Less than 0.2% rms, 1% peak to peak or 50 mV, whichever is greater
9.5.6.4	Voltage Overshoot	-	No greater than 5 %, all outputs
9.5.6.5	Overvoltage Protection	-	130% Vout for all outputs
9.5.6.6	Overload & Short	-	Power foldback point 120% of max rated power
	Circuit Protection	-	Automatic recovery upon removal of fault
9.5.6.7	Inrush Current	-	Cold Start Inrush shall be less than 25A at 115VAC
9.5.6.8	Transient response	-	Output voltage back to within 1% in less than 500 μs on a 50% Load change. Peak transient not to exceed 5%
9.5.6.9	Holdup Time	-	The power supply shall supply 30 watts minimum for 550 ms after ACFAIL going LOW. The supply shall be capable of holding up the Unit for two 500 ms Power Loss periods occurring in a 1.5-second period
9.5.6.10	Remote Sense	-	+5 VDC compensates 250 mV total line drop. Open sense load protection required

CHAPTER 9 SECTION 6

UNIT CHASSIS AND MODEL 2070-5 VME CAGE ASSEMBLY

9.6.1
GENERAL - The Chassis shall consist of the metal housing, Serial Motherboard, Back-plane Mounting Surface, Power Supply Module Supports, slot card guides, Wiring Harnesses, and Cover Plate(s). All external screws shall be countersunk and shall be Phillips flat head stainless steel type. The housing shall be treated with clear chromate and the slot designation labeled on the back-plane mounting surface above the upper slot card guide. The Chassis shall be cooled by convection only. The top and bottom pieces of the housing shall be slotted for vertical ventilation.

9.6.2*
SERIAL MOTHERBOARD shall function as support for its connectors, A1 to A5 and FP, and as the interface between the CPU and the dedicated modules/Front Panel carrying both serial communications, logic, and power circuits. The PCB shall be multi-layered, with one layer plane assigned to DC Ground. A wiring harness PS2 shall be provided between the Model 2070-4 Power Supply and the MOTHERBOARD PCB (provide strain relief). Test points shall be provided on the FPA side of the MOTHERBOARD for PS2 lines. A wiring harness FP shall be provided, linking the MOTHERBOARD with the FPA.

9.6.3
MODEL 2070-5 VME CAGE ASSEMBLY shall consist of 3U five slot/connector VME Cage, Front Mounting Plate, and PS1 Harness. The VME Cage shall conform to VME Standard IEEE P1014/D12 for 3U Cage. All slot/connectors shall be A24: D16 Interface.

9.6.4
The Model 2070 – 1A CPU Main Controller Board shall either be affixed to the Transition Board via at least four stand-off devices or mounted in a one slot VME board assembly (removable). A PS1L Harness shall be supplied with one end mating to the PS1 power supply connector and the other end mated to the MCB DIN Connector. The VME bus lines shall be terminated by a 100-Ohm resistor per line.

CHAPTER 9 SECTION 7

CHAPTER DETAILS

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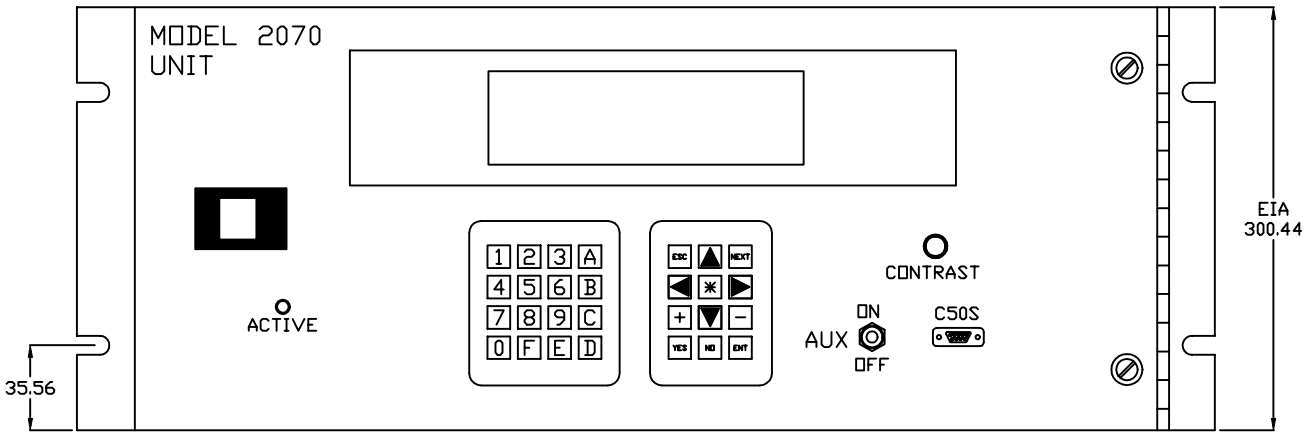
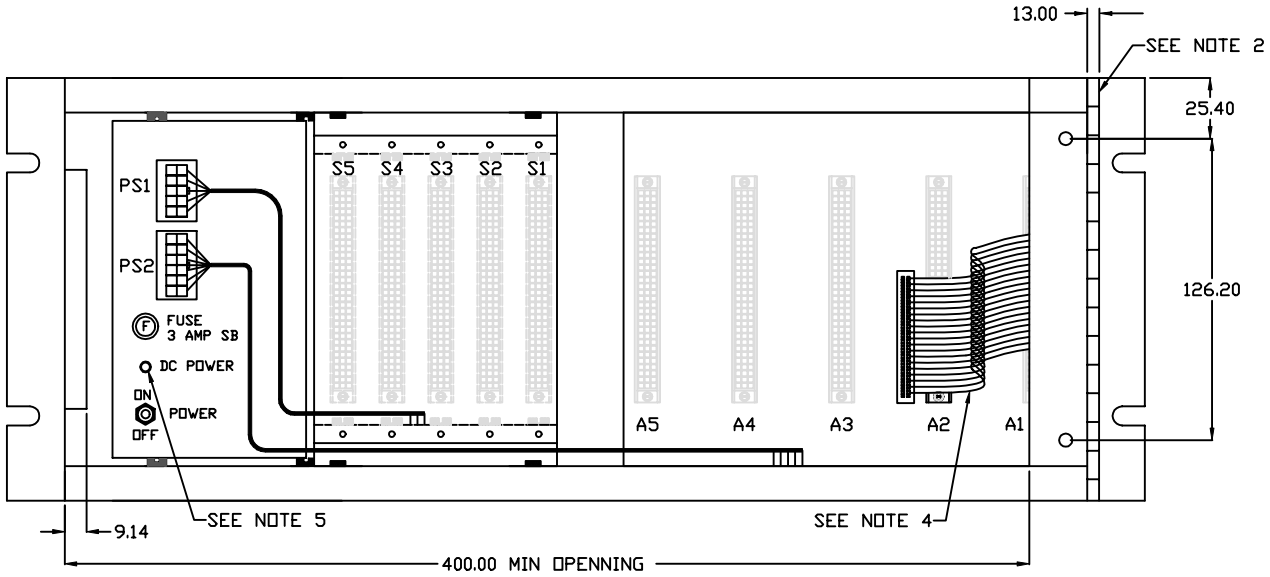
All dimensions are in millimeters.



FRONT PANEL INSTALLED



FRONT PANEL REMOVED

NOTES (THIS DETAIL)

1. The unit shall be capable of mounting to a Standard EIA-310B Rack using 4U open end mounting slots.

2. Continuous stainless steel hinge (4mm maximum hinge barrel) that attaches to the Front Panel by two TSD #1 Thumbscrew devices.

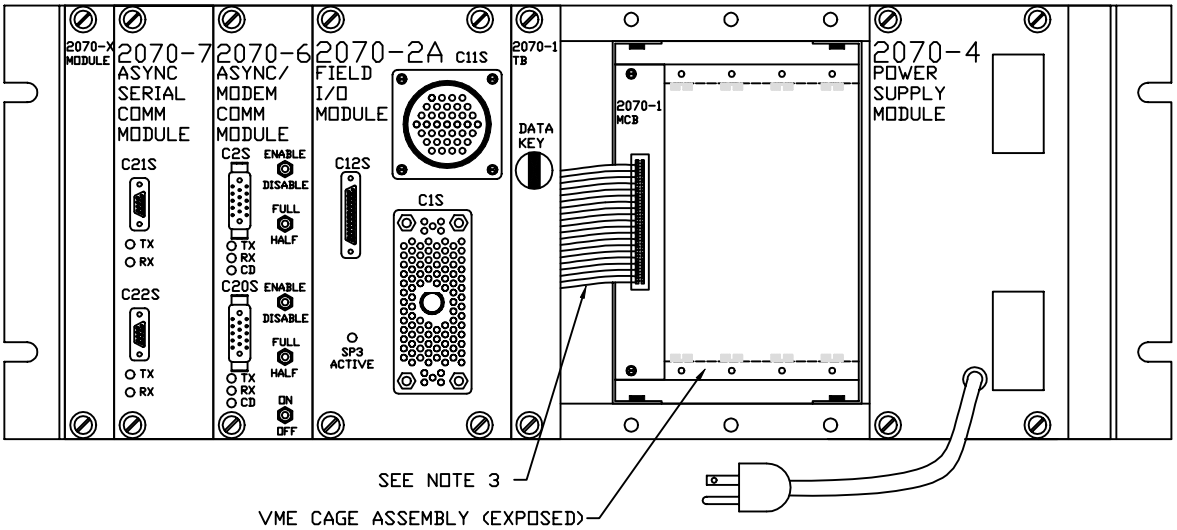
3. Actual location of ACTIVE light and contrast control shall be limited to ACTIVE light on the left side of the panel and the contrast control on the right side. They shall be located greater than 25.4 mm from other devices, connector or latch.

4. The length of the Front Panel Harness shall be no less than 284 mm.

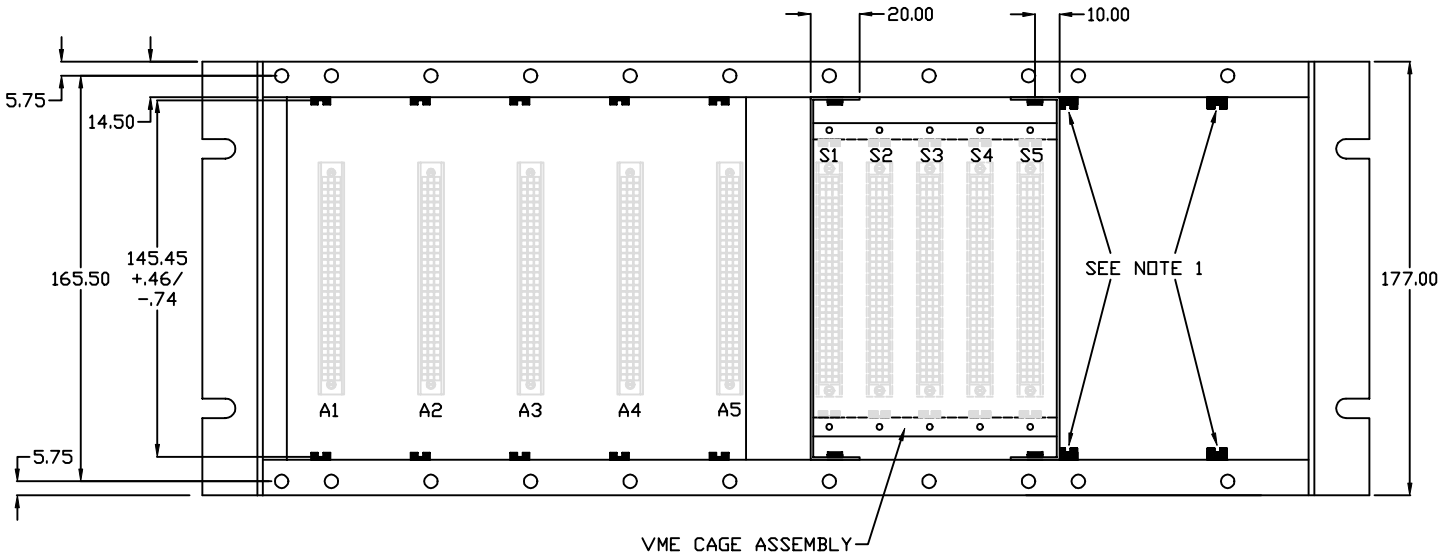
5. A LED indicator for each DC voltage shall be provided.

6. With the hinge installed, the distance between the TSD hole center & the CHASSIS Right Side (inside plane) shall be 14.00 mm

TITLE: MODEL 2070 CHASSIS FRONT VIEW		
	NO SCALE	
	MARCH 29, 2002	9-7-1



REAR VIEW, LOADED



REAR VIEW, UNLOADED

NOTES (THIS DETAIL)

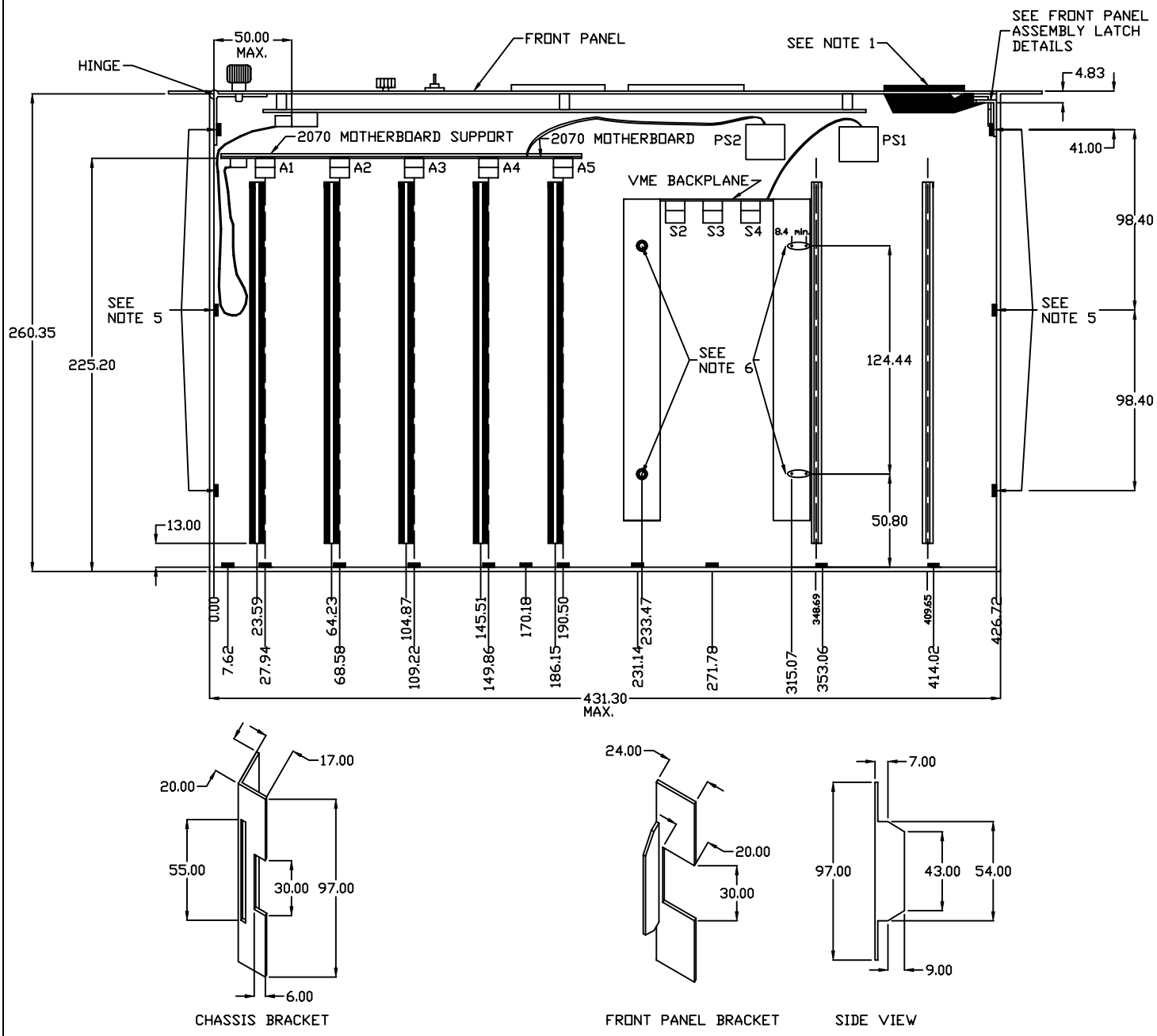
1. Four permanently attached 203.2 mm long Card Guides SAE 1800F (OR EQUAL) beginning 13 mm from the backplane mounting surface.

2. TB - TRANSITION BOARD
   MCB - MAIN CONTROLLER BOARD

3. Maximum length of harness shall be 101.60 mm, and shall not protrude beyond the back of the 2070 unit.

4. The VME Cage Assembly Openning shall be delivered covered by a blank panel. Matching M3 PEM fasteners shall be provided on the back plane surface for panel mounting.

TITLE: MODEL 2070 CHASSIS REAR VIEW		
	NO SCALE	
	MARCH 29, 2002	9-7-2



CHASSIS BRACKET

FRONT PANEL BRACKET

SIDE VIEW

FRONT PANEL ASSEMBLY LATCH DETAILS

NOTES (THIS DETAIL)

1. Front Panel Assembly Latch mating with and rigidly held in place by Chassis Guide Latch/member shall be provided. The member shall vertically support the Front Panel Assembly in two other points besides the Latch.

2. Nylon card guides, SAE 1800F (OR EQUAL), shall be provided (top and bottom) for Mother Slot/Connectors A1 to A5. The Guides shall begin 13 mm from the Backplane surface.

3. M3 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes located on Backplane Surface.

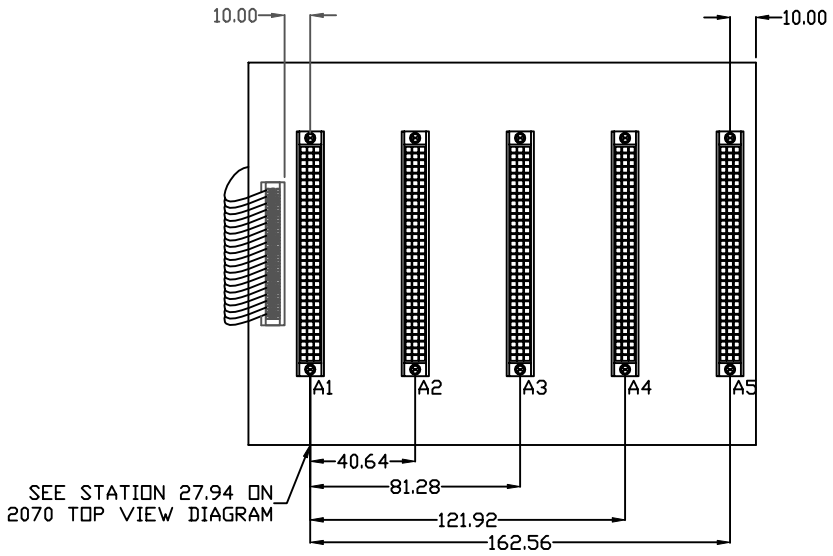
4. All harnesses shall have a minimum slack of 25 mm when connected.

5. M3 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes to match the TSD #3 Thumbscrew Devices on the Model 2070-8 Module. Fastener centers shall be 6.35 mm above unit baseline.

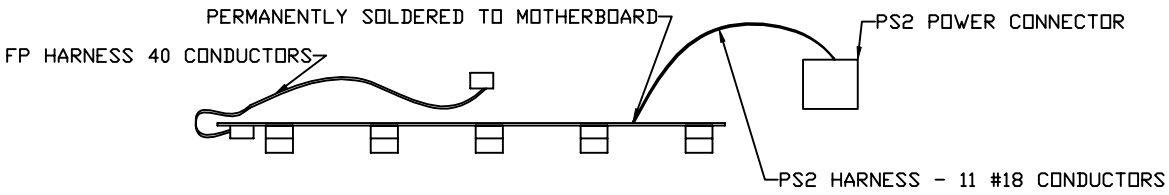
6. Eight 6-32 Phillips head counter-sunk screws, 4 top and 4 bottom, shall be used to mount the cage assembly to the 2070 Chassis.

7. The 2070 chassis top & bottom sections shall be constructed with a continuous 15.77 mm folded lip along the front perpendicular to the 2070 top and bottom sections. The top and bottom sections of the 2070 chassis shall be recessed 18 mm as measured from the front surface of the front panel.

TITLE: MODEL 2070 CHASSIS TOP VIEW		
	NO SCALE	
	MARCH 29, 2002	9-7-3



FRONT VIEW



TOP VIEW

FP HARNESS PIN/WIRING ASSIGNMENT			
PIN	CONNECTOR ROW A	PIN	CONNECTOR ROW B
1	SP4-TXD+	2	SP4-TXD-
3	SP4-RXD+	4	SP4-RXD-
5	SP6-TXD+	6	SP6-TXD-
7	SP6-RXD+	8	SP6-RXD-
9	NA	10	NA
11	NA	12	NA
13	NA	14	NA
15	NA	16	NA
17	NA	18	NA
19	NA	20	NA
21	DC GROUND #1	22	DC GROUND #1
23	+12 VDC SERIAL	24	-12 VDC SERIAL
25	DC GROUND #1	26	DC GROUND #1
27	CPU LED	28	DC GROUND #1
29	CPURESET	30	DC GROUND #1
31	DC GROUND #1	32	C50 ENABLE
33	DC GROUND #1	34	+5 VDC
35	+5 VDC	36	+5 VDC
37	+5 VDC	38	+5 VDC
39	NA	40	NA

PS2 HARNESS PIN/WIRING ASSIGNMENT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SERIAL
3	-12 VDC SERIAL
4	DC GND #1 (+5 VDC & 12 SERIAL)
5	+5 VDC STANDBY
6	+12 VDC - ISOLATED
7	DC GROUND #2 (+12 VDC ONLY)
8	POWER DOWN
9	POWER UP / SYS RESET
10	EQUIPMENT GROUND
11	LINESYNC
12	NA

NOTES (THIS DETAIL)

1. The Motherboard shall be a 3.175 mm minimum thickness pcb mechanically mounted in a vertical position.

2. A1 to A5 receptacle connectors shall be 96 socket contact DIN 41612 connectors (ROBINSON NUGENT #DIN 96RSC or ELCO Series 8477 Three Row Inverted Socket OR EQUAL).

3. The FP Harness may be located on either side of the motherboard. The FP Harness shall either be directly soldered to the motherboard or a header used.

TITLE: MODEL 2070 CHASSIS MOTHERBOARD

	NO SCALE	
	MARCH 29, 2002	9-7-4

A1 CONNECTOR PIN OUT			
PIN	A	B	C
1	SP3TXD+	SP6TXD+	SP5TXD+
2	SP3TXD-	SP6TXD-	SP5TXD-
3	SP3RXD+	SP6RXD+	SP5TXC+
4	SP3RXD-	SP6RXD-	SP5TXC-
5	SP3RTS+	SP3TXC□+	SP5RXD+
6	SP3RTS-	SP3TXC□-	SP5RXD-
7	SP3CTS+	SP3TXCI+	SP5RXC+
8	SP3CTS-	SP3TXCI-	SP5RXC-
9	SP3DCD+	SP3RXC+	SP3TXD+
10	SP3DCD-	SP3RXC-	SP3TXD-
11	SP4TXD+	SP4TXD+	SP3RXD+
12	SP4TXD-	SP4TXD-	SP3RXD-
13	SP4RXD+	SP4RXD+	SP3RTS+
14	SP4RXD-	SP4RXD-	SP3RTS-
15	NA	NA	SP3CTS+
16	NA	NA	SP3CTS-
17	NA	NA	SP3DCD+
18	NA	NA	SP3DCD-
19	NA	NA	SP3TXC□+
20	NA	NA	SP3TXC□-
21	DCG #1	C50 ENABLE	SP3TXCI+
22	NETWK1	NA	SP3TXCI-
23	NETWK2	NA	SP3RXC+
24	NA	LINESYNC	SP3RXC-
25	NETWK3	P□WERUP	CPURESET
26	NETWK4	P□WERDN	FPLED
27	DCG #1	DCG #1	DCG #1
28	+12 SER	-12 SER	+5 STDBY
29	+5 VDC	+5 VDC	+5 VDC
30	DCG #1	DCG #1	DCG #1
31	+12 VDC	+12 VDC	+12 VDC
32	DCG #2	DCG #2	DCG #2

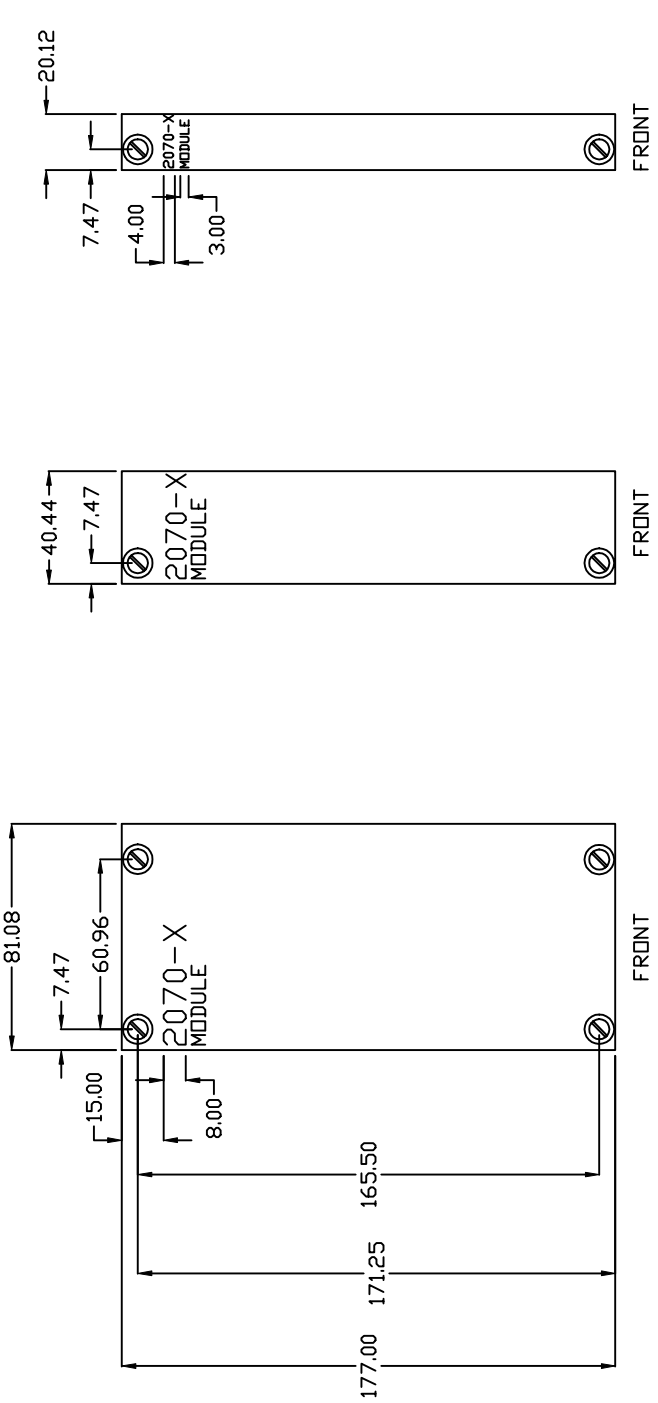
A2 TO A5 CONNECTOR PIN OUT			
PIN	A	B	C
1	SP1TXD+	SP6TXD+	SP5TXD+
2	SP1TXD-	SP6TXD-	SP5TXD-
3	SP1RXD+	SP6RXD+	SP5TXC+
4	SP1RXD-	SP6RXD-	SP5TXC-
5	SP1RTS+	SP1TXC0+	SP5RXD+
6	SP1RTS-	SP1TXC0-	SP5RXD-
7	SP1CTS+	SP1TXCI+	SP5RXC+
8	SP1CTS-	SP1TXCI-	SP5RXC-
9	SP1DCD+	SP1RXC+	SP3TXD+
10	SP1DCD-	SP1RXC-	SP3TXD-
11	SP2TXD+	SP4TXD+	SP3RXD+
12	SP2TXD-	SP4TXD-	SP3RXD-
13	SP2RXD+	SP4RXD+	SP3RTS+
14	SP2RXD-	SP4RXD-	SP3RTS-
15	SP2RTS+	SP2TXC□+	SP3CTS+
16	SP2RTS-	SP2TXC□-	SP3CTS-
17	SP2CTS+	SP2TXCI+	SP3DCD+
18	SP2CTS-	SP2TXCI-	SP3DCD-
19	SP2DCD+	SP2RXC+	SP3TXC□+
20	SP2DCD-	SP2RXC-	SP3TXC□-
21	DCG #1	NA	SP3TXCI+
22	NETWK1	NA	SP3TXCI-
23	NETWK2	NA	SP3RXC+
24	NA	LINESYNC	SP3RXC-
25	NETWK3	P□WERUP	CPURESET
26	NETWK4	P□WERDN	FPLED
27	DCG #1	DCG #1	DCG #1
28	+12 SER	-12 SER	+5 STDBY
29	+5 VDC	+5 VDC	+5 VDC
30	DCG #1	DCG #1	DCG #1
31	+12 VDC	+12 VDC	+12 VDC
32	DCG #2	DCG #2	DCG #2

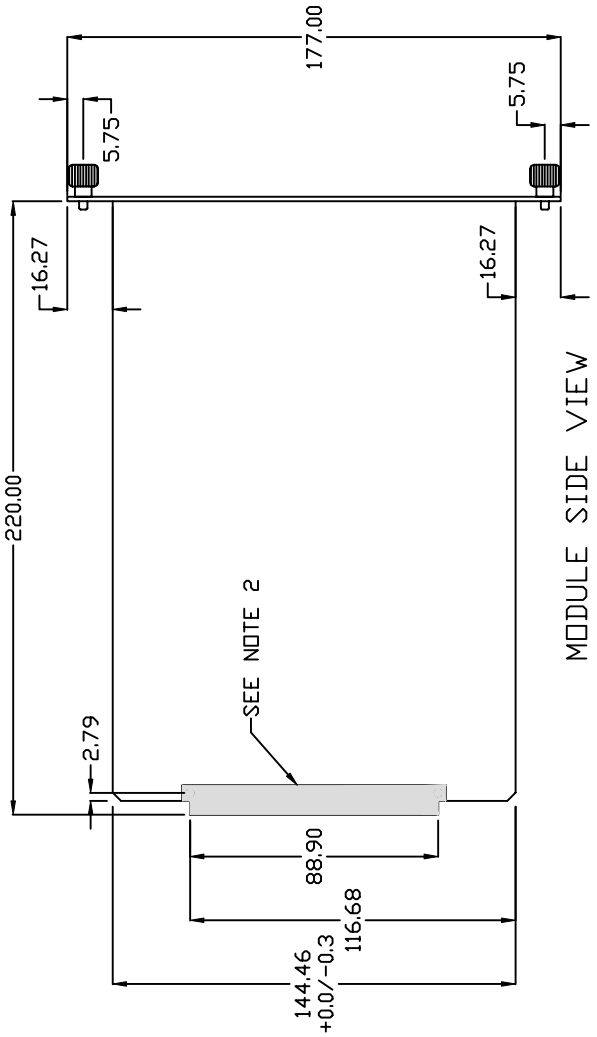
NOTES (THIS DETAIL)

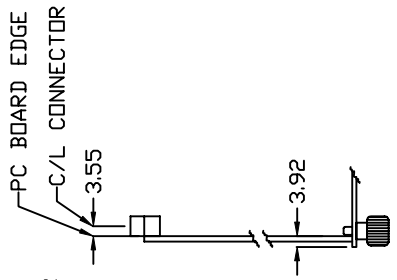
1. Functions are referenced to the CPU.
2. DC GND #1 for +5VDC and +12VDC Serial. DC GND #2 for +12VDC ISO.
3. A1 Connector is the furthest A Connector to the left when viewed from the unit back. All A Connectors are pin assigned the same.
4. Connector A2 to A4, pins B21 and B22 shall read "NA".
   Connector A2, pins B23 shall read "A2 Installed".
   Connector A3, pins B23 shall read "A3 Installed".
   Connector A4, pins B23 shall read "NA".
   Connector A5, pins B21 shall read "A2 Installed".
   Connector A5, pins B22 shall read "DCG #1".
   Connector A5, pins B23 shall read "A3 Installed".
5. Pin A24 (DCG #1) is reserved for network protection only, ie., "Ethernet Shield".
6. Connector A2 installed, enables SP1 and SP2.
7. Connector A3 install, enbales SP5.
8. SP3 and SP6 are always enabled.
9. C50 enabled, disconnects SP4 on connector A1.

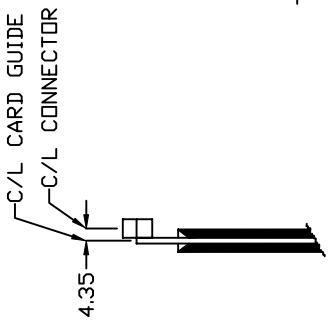
TITLE:
Motherboard A Connector Pin Assignment

NO SCALE	
MARCH 29, 2002	9-7-5









TOP VIEW DETAILS

NOTES (THIS DETAIL)

1. All Thumbscrew devices on modules described in this drawing shall be TD#3 OR EQUAL.
2. 96 pin DIN connector ELCO # 00 8272 96 000 013 OR EQUAL.

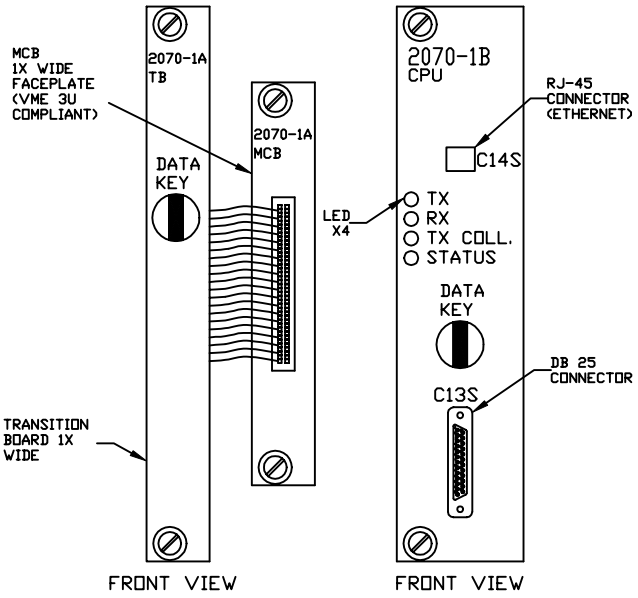
TITLE: MODEL 2070 SYSTEM PCB MODULES, GENERAL

	NO SCALE	
	MARCH 29, 2002	9-7-6

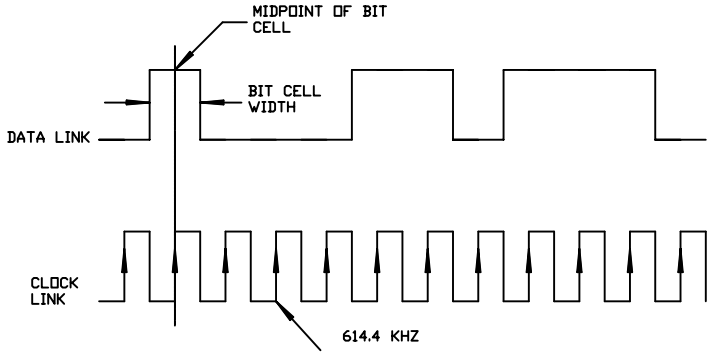
SERIAL PORT REQUIREMENTS

A2 TO A5 CONNECTOR PIN OUT			
LOGICAL PORT	68360 PORT	RATE KBITS	PROTOCOL
SP1	SEE NOTE 4	(1)	ASYNC
SP1S	SEE NOTE 4	(2)	SYNC, HDLC, SDLC
SP2	SCC2	(1)	ASYNC
SP2S	SCC2	(2)	SYNC, HDLC, SDLC
SP3	SCC4	(1)	ASYNC
SP3S	SCC4	153.6, 614.4*	SYNC, HDLC, SDLC
SP4	SMC2	(1)	ASYNC
SP5	SCC3	(1)	ASYNC
SP5S	SCC3	153.6, 614.4*	SYNC, HDLC, SDLC
SP6	SMC1	(1), 38.4*	ASYNC

SDLC FRAME LAYOUT					
OPENNING FLAG	ADDR	CONTROL	INFORMATION	CRC	CLOSING FLAG
0111 1110	8 BITS	1000 0011	VARIABLE LENGTH	16 BITS	0111 1110



CPU FACE PANELS



SDLC TIMING

C13S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	SP8 TX +	14	SP8 TX -
2	SP8 RX +	15	SP8 RX -
3	SP8 TXC +	16	SP8 TXC -
4	SP8 RXC +	17	SP8 RXC -
5	SP8 RTS + **	18	SP8 RTS - **
6	SP8 CTS + **	19	SP8 CTS - **
7	SP8 DCD + **	20	SP8 DCD - **
8	NA	21	NA
9	LINESYNC +	22	LINESYNC -
10	NRESET +	23	NRESET -
11	PWRDWN +	24	PWRDWN -
12	+5 VDC	25	EQUIP GND
13	DC GND #2		

C14S PIN ASSIGNMENT (ETHERNET)			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

NOTES (THIS DETAIL)

1. (1) BPS Rates 1.2* 2.4, 4.8, 9.6, 19.2, 38.4

2. (2) BPS Rates 19.2*, 38.4, 57.6, 76.8, 153.6

3. * Default BPS Rate for indicated Port.
   ** Disconnected by internal switch.

4. SP1 OF THE 2070-1A is 68360 SCC1. SP1 OF THE 2070-1B is Dual SCC1 with 68360 SCC1 assigned to ETHERNET.

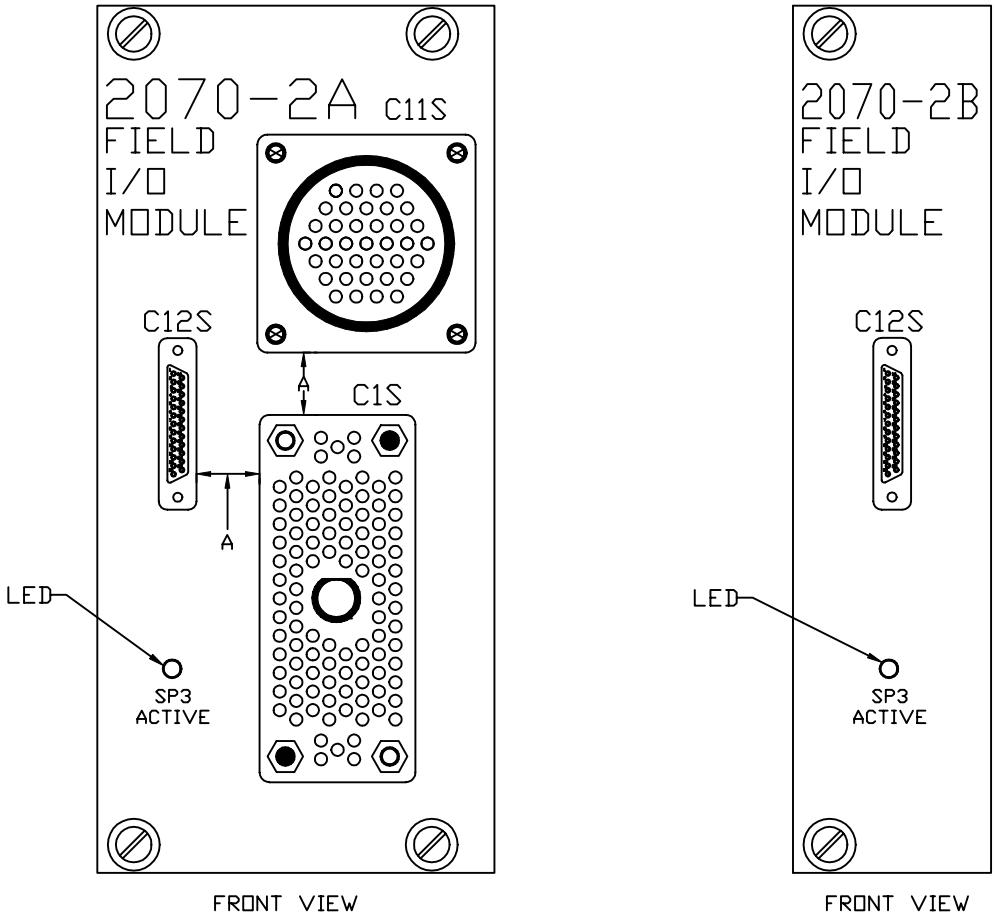
5. A Post Header (ROBINSON NUGENT IDA-XX OR EQUAL) Connector with strain relief shall be provided on the MCB Front Plate and the Transition Board for mating with the interface harness. The harness shall be shielded and straight through wired.

TITLE: MODEL 2070-1 CPU MODULES AND SERIAL PORT/SDLC PROTOCOL

NO SCALE

MARCH 29, 2002

9-7-7



FIELD I/O FACE PANELS

NOTES (THIS DETAIL)

1. 2070-2A Faceplate shall be 4X wide. 2070-2B Faceplate shall be 2X wide. (SEE SYSTEM PCB MODULE, GENERAL DETAILS.)

2. Dark Circles in the C1S Connector denote guide pin locations and open circles denote guide socket locations.

3. Dimension "A" shall be a minimum of 12.7 mm.

4. C1S - M104 Type
   C11S - 37-Pin Circular Plastic Type
   C12S - 25-Pin DB Socket Type

5. C12S PIN 12 (+5VDC) IS DERIVED from +12 VDC Power Supply

C12S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	TX5 DATA +	14	TX5 DATA -
2	RX5 DATA +	15	RX5 DATA -
3	TX5 CLOCK +	16	TX5 CLOCK -
4	RX5 CLOCK +	17	RX5 CLOCK -
5	TX3 DATA +	18	TX3 DATA -
6	RX3 DATA +	19	RX3 DATA -
7	TX3 CLOCK +	20	TX3 CLOCK -
8	RX3 CLOCK +	21	RX3 CLOCK -
9	LINE SYNC +	22	LINE SYNC -
10	NRESET +	23	NRESET -
11	POWER DOWN +	24	POWER DOWN -
12	+5 VDC	25	EQUIP GND
13	DC GND #2		

TITLE:

MODEL 2070-2
FIELD I/O MODULES

NO SCALE	
MARCH 29, 2002	9-7-8

C1S PIN ASSIGNMENT

PIN	FUNCTION	
	NAME	PORT
1	DC GROUND	
2	O0	O1-1
3	O1	O1-2
4	O2	O1-3
5	O3	O1-4
6	O4	O1-5
7	O5	O1-6
8	O6	O1-7
9	O7	O1-8
10	O8	O2-1
11	O9	O2-2
12	O10	O2-3
13	O11	O2-4
14	DC GROUND	
15	O12	O2-5
16	O13	O2-6
17	O14	O2-7
18	O15	O2-8
19	O16	O3-1
20	O17	O3-2
21	O18	O3-3
22	O19	O3-4
23	O20	O3-5
24	O21	O3-6
25	O22	O3-7
26	O23	O3-8

PIN	FUNCTION	
	NAME	PORT
27	O24	O4-1
28	O25	O4-2
29	O26	O4-3
30	O27	O4-4
31	O28	O4-5
32	O29	O4-6
33	O30	O4-7
34	O31	O4-8
35	O32	O5-1
36	O33	O5-2
37	O34	O5-3
38	O35	O5-4
39	I0	I1-1
40	I1	I1-2
41	I2	I1-3
42	I3	I1-4
43	I4	I1-5
44	I5	I1-6
45	I6	I1-7
46	I7	I1-8
47	I8	I2-1
48	I9	I2-2
49	I10	I2-3
50	I11	I2-4
51	I12	I2-5
52	I13	I2-6

PIN	FUNCTION	
	NAME	PORT
53	I14	I2-7
54	I15	I2-8
55	I16	I3-1
56	I17	I3-2
57	I18	I3-3
58	I19	I3-4
59	I20	I3-5
60	I21	I3-6
61	I22	I3-7
62	I23	I3-8
63	I28	I4-5
64	I29	I4-6
65	I30	I4-7
66	I31	I4-8
67	I32	I5-1
68	I33	I5-2
69	I34	I5-3
70	I35	I5-4
71	I36	I5-5
72	I37	I5-6
73	I38	I5-7
74	I39	I5-8
75	I40	I6-1
76	I41	I6-2
77	I42	I6-3
78	I43	I6-4

PIN	FUNCTION	
	NAME	PORT
79	I44	I6-5
80	I45	I6-6
81	I46	I6-7
82	I47	I6-8
83	O40	O6-1
84	O41	O6-2
85	O42	O6-3
86	O43	O6-4
87	O44	O6-5
88	O45	O6-6
89	O46	O6-7
90	O47	O6-8
91	O48	O7-1
92	DC GROUND	
93	O49	O7-2
94	O50	O7-3
95	O51	O7-4
96	O52	O7-5
97	O53	O7-6
98	O54	O7-7
99	O55	O7-8
100	O36	O5-5
101	O37	O5-6
102	O38 DET RES	O5-7
103	O39 WDT	O5-8
104	DC GROUND	

C11S PIN ASSIGNMENT

PIN	FUNCTION	
	NAME	PORT
1	O56	O8-1
2	O57	O8-2
3	O58	O8-3
4	O59	O8-4
5	O60	O8-5
6	O61	O8-6
7	O62	O8-7
8	O63	O8-8
9	DC GROUND	
10	I24	I4-1

PIN	FUNCTION	
	NAME	PORT
11	I25	I4-2
12	I26	I4-3
13	I27	I4-4
14	DC GROUND	
15	I48	I7-1
16	I49	I7-2
17	I50	I7-3
18	I51	I7-4
19	I52	I7-5
20	I53	I7-6

PIN	FUNCTION	
	NAME	PORT
21	I54	I7-7
22	I55	I7-8
23	I56	I8-1
24	I57	I8-2
25	I58	I8-3
26	I59	I8-4
27	I60	I8-5
28	I61	I8-6
29	I62	I8-7
30	I63	I8-8

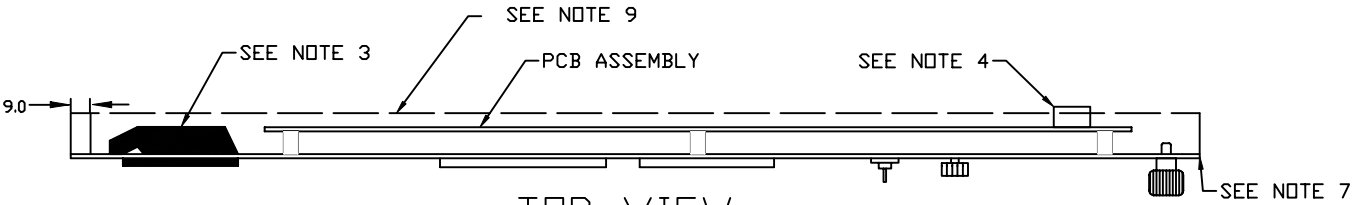
PIN	FUNCTION	
	NAME	PORT
31	DC GROUND	
32	NA	- - -
33	NA	- - -
34	NA	- - -
35	NA	- - -
36	NA	- - -
37	DC GROUND	

TITLE: MODEL 2070-2A
FIELD I/O MODULE
C1 & C11 CONNECTORS

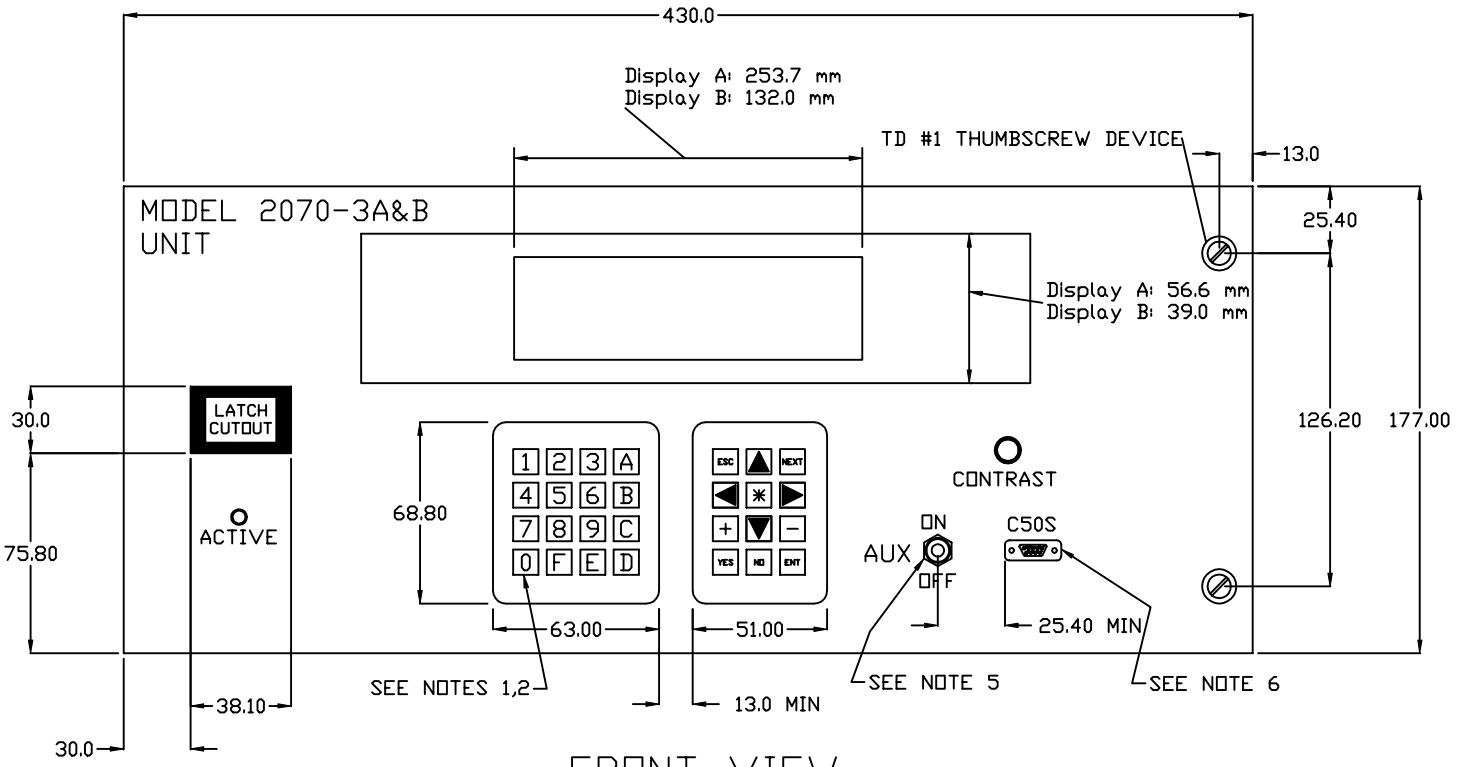
NO SCALE

MARCH 29, 2002

9-7-9



TOP VIEW



FRONT VIEW

NOTES (THIS DETAIL)

1. Key size shall be 7.62 X 7.62.
2. Key center to center spacing shall be 12.70 mm.
3. Slide latch shall be a SOUTHCO flush style A3-40-625-12 (OR EQUAL).
4. 40 contact FP harness pin header connector. It shall be compatible to the FP harness in type and pin assignments. Center of the FP harness header shall be vertically positioned 90 +/- 5 mm as measured from the top of the FPA.
5. Two position CONTROL switch mounted vertically.
6. "C50S" connector shall be a DB-9 socket contact connector.
7. Front panel sheet metal thickness shall be 1.52 ±0.13.
8. All FPA devices shall be located as shown.
9. The FPA shall be provided with a continuous top and bottom 17 mm lip bent 90 degrees to the front plate and shall extend the full length of the FPA.

C50S CONNECTOR PINOUTS	
PIN	C50S FUNCTION
1	C50 ENABLE
2	SP4 RX
3	SP4 TX
4	NA
5	DC GROUND #1
6	NA
7	NA
8	NA
9	NA

C60S CONNECTOR PINOUTS	
PIN	FUNCTION
1	NA
2	SP6 RX
3	SP6 TX
4	NA
5	DC GROUND #1
6	NA
7	CPU RESET
8	NA
9	CPU LED

TITLE:

MODEL 2070-3A&B FRONT PANEL ASSEMBLY

	NO SCALE	
	MARCH 29, 2002	9-7-10

MODEL 2070-3 AUX SWITCH CODES		
SWITCH POSITION	ASCII DATA (TEXT)	ASCII DATA (HEX)
ON	ESC O T	1B 4F 54
OFF	ESC O U	1B 4F 55

MODEL 2070-3 KEY CODES		
KEY	ASCII DATA (TEXT)	ASCII DATA (HEX)
0	0	30
1	1	31
2	2	32
3	3	33
4	4	34
5	5	35
6	6	36
7	7	37
8	8	38
9	9	39
A	A	41
B	B	42
C	C	43
D	D	44
E	E	45
F	F	46
(UP ARROW)	ESC [A	1B 5B 41
(DOWN ARROW)	ESC [B	1B 5B 42
(RIGHT ARROW)	ESC [C	1B 5B 43
(LEFT ARROW)	ESC [D	1B 5B 44
ESC	ESC O S	1B 4F 53
NEXT	ESC O P	1B 4F 50
YES	ESC O Q	1B 4F 51
NO	ESC O R	1B 4F 52
*	*	2A
+	+	2B
-	-	2D
ENTER	CR	OD

TITLE:

MODEL 2070-3
FRONT PANEL ASSEMBLY
KEY CODES

NO SCALE

MARCH 29, 2002

9-7-11

CONFIGURATION COMMAND CODES

ASCII REPRESENTATION	HEX VALUE	FUNCTION
HT	09	Move cursor to next tab stop
CR	0D	Position cursor at first position on current line
LF	0A	(Line Feed) Move cursor down one line
BS	08	(Backspace) Move cursor one position to the left and write space
ESC [Py ; Px f	1B 5B Py 3B Px 66	Position cursor at (Px, Py)
ESC [Pn C	1B 5B Pn 43	Position cursor Pn positions to right
ESC [Pn D	1B 5B Pn 44	Position cursor Pn positions to left
ESC [Pn A	1B 5B Pn 41	Position cursor Pn positions up
ESC [Pn B	1B 5B Pn 42	Position cursor Pn positions down
ESC [H	1B 5B 48	Home cursor (move to 1,1)
ESC [2 J	1B 5B 32 4A	Clear screen with spaces without moving cursor
ESC c	1B 63	Soft reset
ESC P P1 [Pn ; Pn...f	1B 50 P1 5B Pn 3B...Pn 66	Compose special character number Pn (1-8) at current cursor position
ESC [< Pn V	1B 5B 3C Pn 56	Display special character number Pn (1-8) at current cursor position
ESC [25 h	1B 5B 32 35 68	Turn Character blink on
ESC [25 l	1B 5B 32 35 6C	Turn character blink off
ESC [< 5 h	1B 5B 3C 35 68	Illuminate Backlight
ESC [< 5 l	1B 3B 3C 35 6C	Extinguish Backlight
ESC [33 h	1B 5B 33 33 68	Cursor blink on
ESC [33 l	1B 5B 33 33 6C	Cursor blink off
ESC [27 h	1B 5B 32 37 68	Reverse video on -Note 2
ESC [27 l	1B 5B 32 37 6C	Reverse video off -Note 2
ESC [24 h	1B 5B 32 34 68	Underline on -Note 2
ESC [24 l	1B 5B 32 34 6C	Underline off -Note 2
ESC [0 m	1B 5B 30 6D	All attributes off
ESC H	1B 48	Set tab stop at current cursor position
ESC [Pn g	1B 5B Pn 67	Clear tab stop Pn = 0,1,2 at cursor = 3 all tab stops
ESC [? 7 h	1B 5B 3F 37 68	Auto-wrap on
ESC [? 7 l	1B 5B 3F 37 6C	Auto-wrap off
ESC [? 8 h	1B 5B 3F 38 68	Auto-repeat on
ESC [? 8 l	1B 5B 3F 38 6C	Auto-repeat off
ESC [? 25 h	1B 5B 3F 32 35 68	Cursor on
ESC [? 25 l	1B 5B 3F 32 35 6C	Cursor off
ESC [< 47 h	1B 5B 3C 34 37 68	Auto-scroll on
ESC [< 47 l	1B 5B 3C 34 37 6C	Auto-scroll off
ESC [< Pn S	1B 5B 3C Pn 53	Set Backlight timeout value to Pn (0-63)
ESC [PU	1B 5B 50 55	String sent to CPU when FPA power up

NOTE: 1. Numerical values have one ASCII character per digit without leading zero.
2. Reverse Video & Underline NOT required for Front Panel Assembly Option 3A & B. Commends shall be available for option 3C (C60).

INQUIRY COMMAND-RESPONSE CODES

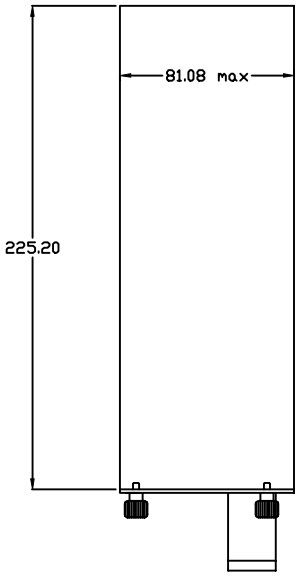
COMMAND CPU Module to Front Panel Module		RESPONSE Front Panel Module to CPU Module		FUNCTION
ASCII Representation	HEX Value	ASCII Representation	HEX Value	
ESC [6 n	1B 5B 36 6E	ESC [Py; Px R	1B 5B Py 3B Px 52	Inquire Cursor Position
ESC [B n	1B 5B 42 6E	ESC [P1;P2;.....P6 R	1B 5B P1 3B P2 3B....P6 52	Status Cursor Position P1: Auto-wrap (h,l) P2: Auto-scroll (h,l) P3: Auto-repeat (h,l) P4: Backlight (h,l) P5: Backlight timeout P6: AUX Switch (h,l)
ESC [A n	1B 5B 41 6E	ESC [P1 R	1B 5B P1 52	P1: AUX Switch (h,l)

TITLE: MODEL 2070-3 FRONT PANEL ASSEMBLY KEY CODES

NO SCALE

MARCH 29, 2002

9-7-12



TOP VIEW

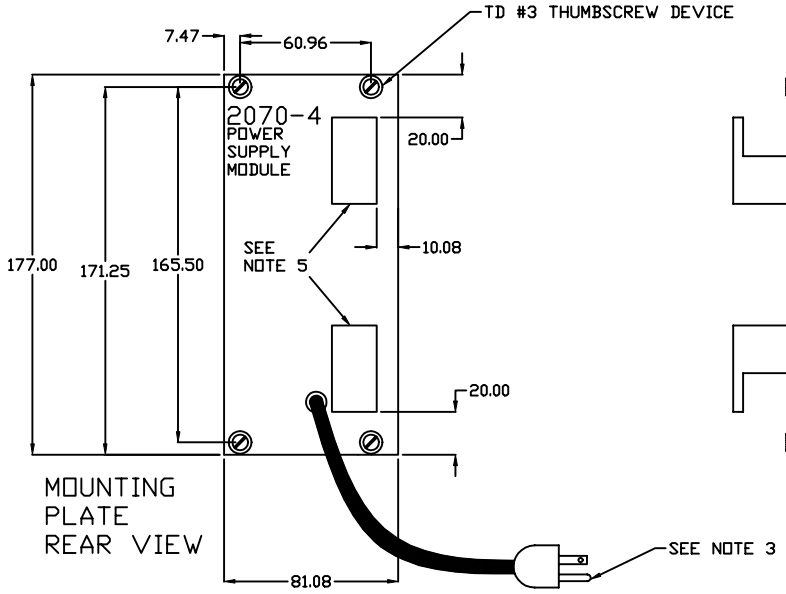
PS1 CONNECTOR PINOUT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SERIAL
3	-12 VDC SERIAL
4	DC GND #1 (+5 VDC & 12 SERIAL)
5	+5 VDC STANDBY
6	+5 VDC SENSE
7	DC GROUND SENSE
8	AC FAIL (VME)
9	SYSRESET (VME)
10	NA

PS2 CONNECTOR PINOUT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SERIAL
3	-12 VDC SERIAL
4	DC GND #1 (+5 VDC & 12 SERIAL)
5	+5 VDC STANDBY
6	+12 VDC
7	DC GROUND (+12 VDC ONLY)
8	POWER DOWN / AC FAIL
9	POWER UP / SYS RESET
10	EQUIPMENT GROUND
11	LINESYNC
12	NA

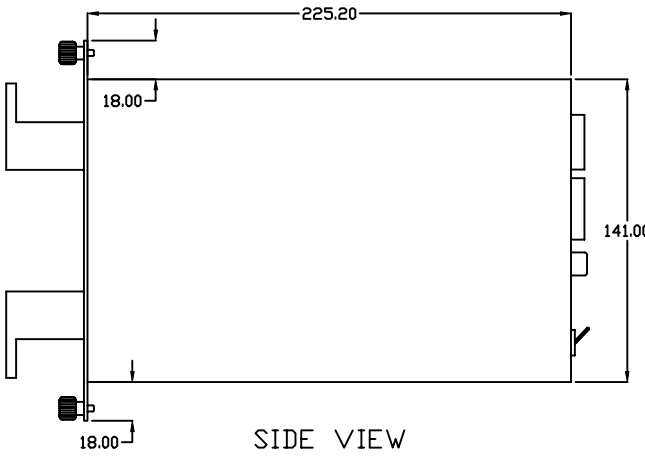
NOTES (THIS DETAIL)

1. Power switch shall be mounted vertically. Power On shall be in the up position.
2. Fuse shall be a replaceable 3AG Slow Blow type resident in a fuse holder. Fuse label shall indicate rating.
3. Three #16 conductor power cable, 1 meter minimum length and permanenlty attached to the Module with strain relief. The end plug connector shall be a three blade NEMA 5-15P grounding plug type.
4. PS1 and PSS2 Receptacle Connectors shall be AMP Mini-Universal Double row MATE-N-LOK CAP Connectors with locking latch devices (OR EQUAL).

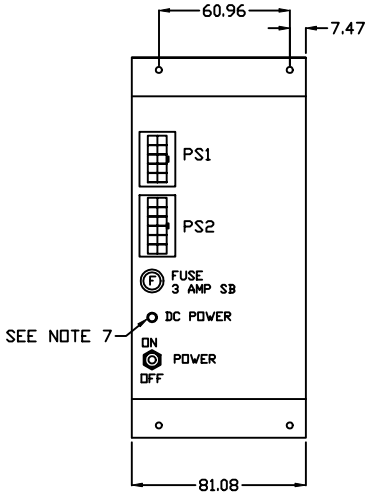
   PS1 connector shall be a 10 position PLUG connector. PS2 connector shall be a 12 position PLUG connector.
5. Buckeye Cord-Wrap PP-40055 device with PP-40058 Extension (OR EQUAL).
6. Mounting Plate shall conform to the 4X Wide Module dimensions.
7. A LED indicator shall be provided for each DC power source (+5, +12 ISO, +12 SERIAL, -12 SERIAL).



MOUNTING
PLATE
REAR VIEW



SIDE VIEW



FRONT VIEW

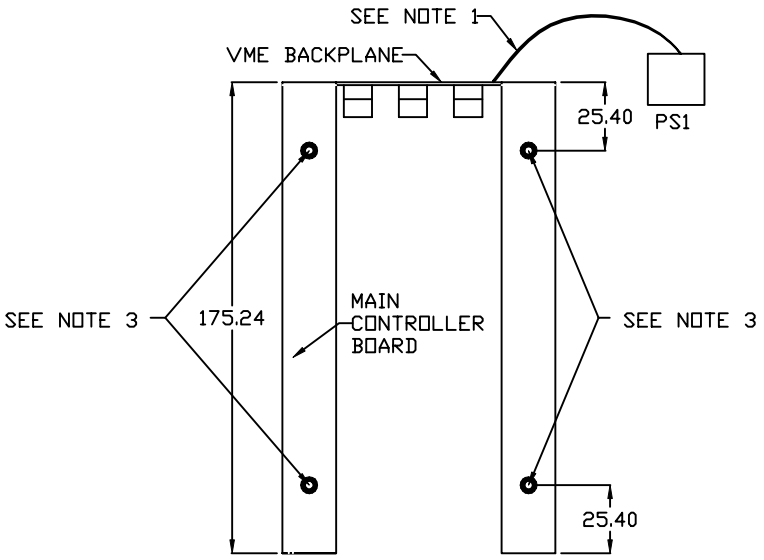
TITLE:

MODEL 2070-4
POWER SUPPLY MODULE

NO SCALE

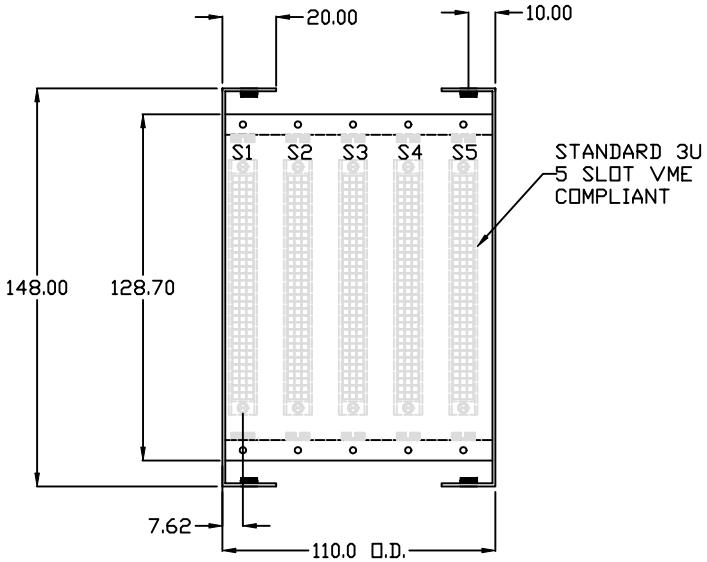
MARCH 29, 2002

9-7-13



TOP VIEW

PS1 CONNECTOR PIN ASSIGNMENT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SERIAL
3	-12 VDC SERIAL
4	DC GND #1 (+5 VDC & 12 SERIAL)
5	+5 VDC STANDBY
6	+5 VDC SENSE
7	DC GROUND SENSE
8	AC FAIL (VME)
9	SYSRESET (VME)
10	NA



FRONT VIEW

NOTES (THIS DETAIL)

1. PS1 Harness interfaces between the Model 2070-4 Power Supply Module and the 2070-5 VME Cage Assembly. The harness shall be permanently attached to the Cage Assembly by solder, FASTON or Power Bugs. The Harness wiring shall be 8 #18 conductors for power and 2 #22 conductors for others.

2. The plate shall cover the open area & attach to the Chassis Backplane mounting surface via screws meeting the Chapter 1 external screw requirements. The screws shall mate with the PEM nuts as specified in the Model 2070 Chassis Top View Detail.

3. G-32 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes to match the 6-32 screws on the top and bottom of the Model 2070 chassis.

TITLE:

MODEL 2070-5
VME CAGE ASSEMBLY

	NO SCALE	
	MARCH 29, 2002	9-7-14

CHAPTER 10

SPECIFICATION FOR MODEL 2070 PERIPHERAL EQUIPMENT

TABLE OF CONTENTS

GENERAL NOTES:

1. **The 2070-6x and 2070-7x modules shall provide circuitry to disable its Channel 2 and EIA 232 control lines when a ground-true state is presented at Connector A1 Pin B21 (C50 Enable). The Disable line shall be pulled up on the module.**
2. **Line drivers/receivers shall be socket or surface mounted.**
3. **Isolation circuitry shall be opto- or capacitive-coupled isolation technologies. Each module's circuit shall be capable of reliably passing a minimum of 1.0 Mbps.**
4. **The Comm modules shall be "Hot" swappable without damage to circuitry or operations.**

CHAPTER 10 SECTION 1

MODEL 2070-6 A & B ASYNC/MODEM SERIAL COMM MODULES

10.1.1
A fused isolated +5 VDC with a minimum of 100 mA power supply shall be provided for external use.

10.1.2
One shall be used to vertically switch between Half Duplex (Down) and Full-Duplex (Up). In Half-Duplex mode, the Transmit connections shall be used for both Receive and Transmit.

10.1.3
Two circuits designated CIRCUIT #1 and CIRCUIT #2, shall be provided. Both circuit functions shall be identical, except for their Serial Communications Port and external connector (CIRCUIT #1 to SP1 [or SP3] and C2S Connector and CIRCUIT #2 to SP2 [or SP4] and C20S Connector). The Circuits shall convert the 2070 UNIT Motherboard SP EIA-485 signals to/from board TTL level signals, isolate and drive the converted EIA-232 Signals interfacing with their associated MODEM and external connector.

10.1.3.1
Each CIRCUIT shall have a MODEM with the following requirements:

1. **Data Rate: Baud modulation of 300 to 1200 for Module 2070-6A and 0 to 9600 for Module 2070-6B.**
2. **Modulation: Phase coherent frequency shift keying (FSK).**
3. **Data Format: Asynchronous, serial by bit.**
4. **Line & Signal Requirements: Type 3002 voice-grade, unconditioned Tone Carrier Frequencies (Transmit and Receive): 2070-6A - 1.2 KHz MARK and 2.2 KHz SPACE, ±1% tolerance. 2070-6B - 11.2 KHz MARK and 17.6 KHz SPACE, ±1% tolerance. The operating band shall be (half power, -3 dB) between 1.0 KHz & .4 KHz for 2070-6A and 9.9 KHz & 18.9 KHz for 2070-6B.**
5. **Transmitting Output Signal Level: 0, -2, -4, -6, and -8 dB (at 1.7 KHz for 2070-6A & 14.7 KHz for 2070-6B) continuous or switch selectable.**
6. **Receiver Input Sensitivity: 0 to -40 dB.**
7. **Receiver Bandpass Filter: Shall meet the error rate requirement specified below and shall provide 20 dB/octave, minimum active attenuation for all frequencies outside the operating band.**
8. *** Clear-to-Send (CTS) Delay: 11 ±3 ms.**
9. **Receive Line Signal Detect Time: 8 ±2 ms mark frequency.**
10. **Receive Line Squelch: 6.5 (±1) ms, 0 ms (OUT).**
11. *** Soft Carrier Turn Off Time: 10 ±2 ms (0.9 KHz for 2070-6A and 7.8 KHz for 2070-6B). When the RTS is unasserted, the carrier shall turn off or go to soft carrier frequency.**
12. **Modem Recovery Timer: Capable of receiving data within 22 ms after completion of transmission.**

13. **Error Rate: Shall not exceed 1 bit in 100 Kbits, with a signal-to-noise ratio of 16 dB measured with flat-weight over a 300 to 3,000 Hz band.**
14. **Transmit Noise: Less than -50 dB across 600-ohms resistive load within the frequency spectrum of 300 to 3,000 Hz at maximum output.**
15. **Modem interface: EIA-232 Standards.**

CHAPTER 10 SECTION 2

MODEL 2070-7A & 7B ASYNC / SYNC SERIAL COMM MODULE

10.2.1
Two circuits designated CIRCUIT #1 and CIRCUIT #2, shall be provided. Their functions are identical, except for the CPU Serial Communications Port and external connector (CIRCUIT #1 to SP1 [or SP3] and Connector C21S and CIRCUIT #2 to SP2 [or SP4] and Connector C22S).

10.2.2
2070 -7A Each circuit shall convert its EIA-485 signal lines (RX, TX, RTS, CTS and DCD) to/from board TTL Level Signals; isolate both signal and ground; and drive / receive external EIA-232 devices via C21 / C22 Connectors. Connectors shall be DB-9S type.

10.2.3
2070 - 7B Each circuit EIA -485 signal lines, (RX, TX, TXC (I), TXC (O) and RXC) and associated signal ground shall be board terminated to matching drivers/receivers; isolated both signal and ground, and drive/receiver external EIA-485 devices via C21/C22 Connectors. Connectors shall be DB-15S type.

10.2.4
Each circuit signal TX and RX line shall have an LED Indicator mounted on the front plate and labeled to function.

CHAPTER 10 SECTION 3

RESERVED FOR MODEL 2070-6D FIBER OPTIC MODULE

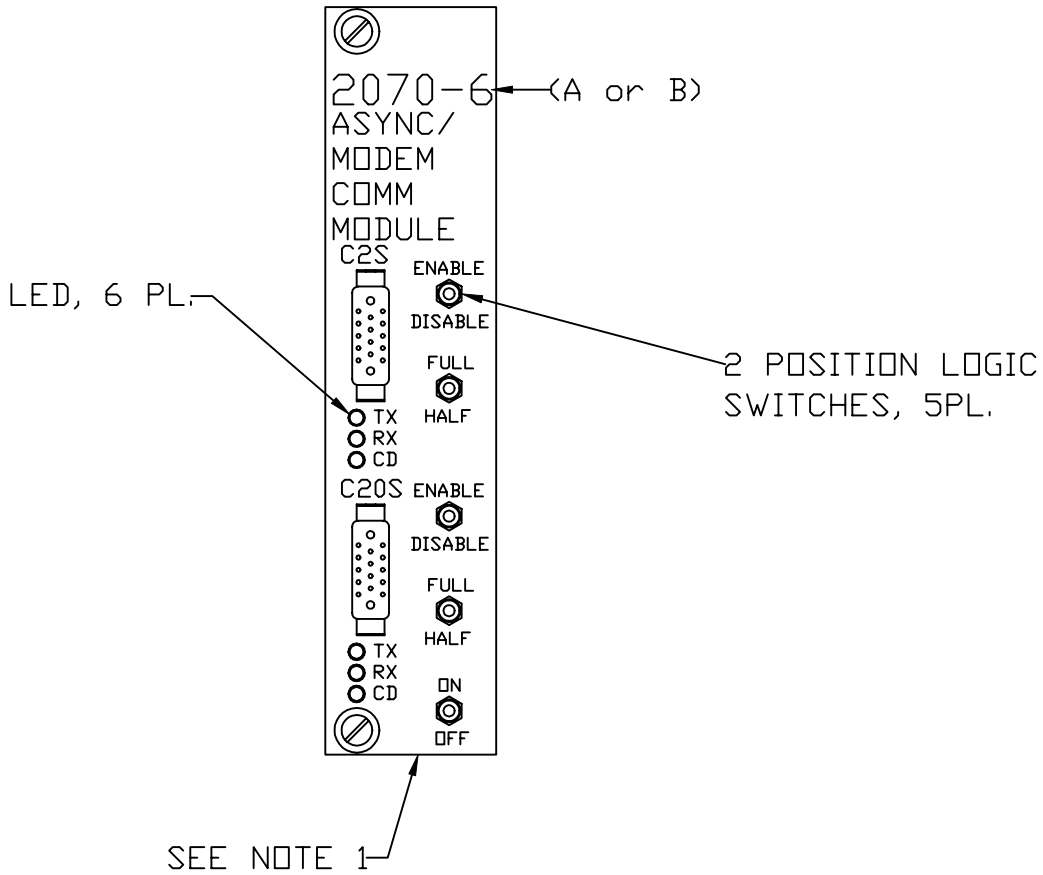
USE CURRENT MODEMS AS HOUSTON SPECIFICATION – FUTURE

Manufactures:

EAGLE
GDI
FORCE (Washington D.C.)
IR DEVICES

CHAPTER 10 SECTION 4

RESERVED FOR MODEL 2070-6E ETHERNET COMMUNICATIONS



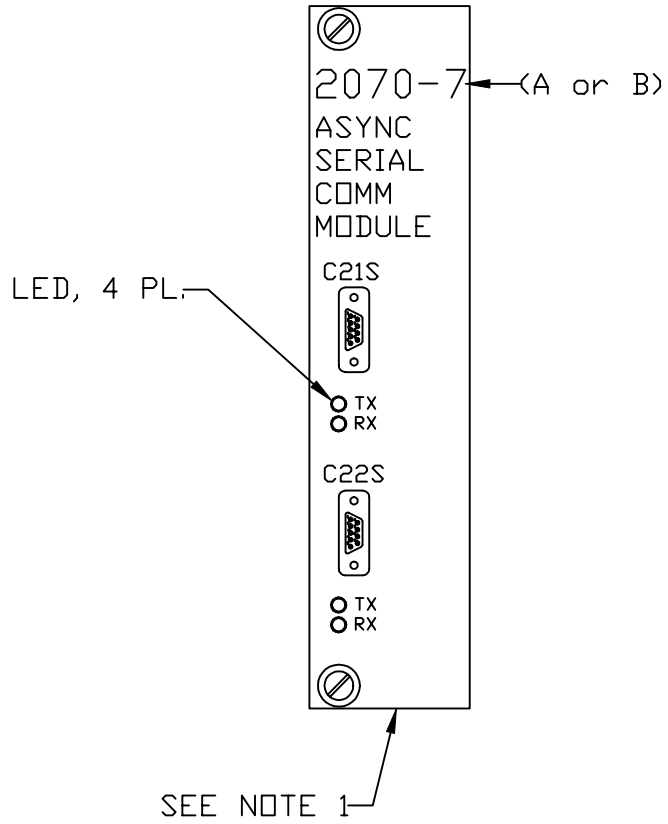
C2 & C20 CONNECTOR PINOUT			
PIN	FUNCTION	PIN	FUNCTION
A	AUDIO IN	J	RTS
B	AUDIO IN	K	DATA IN
C	AUDIO OUT	L	DATA OUT
D	ISO +5 VDC	M	CTS
E	AUDIO OUT	N	ISO DC GND
F	NA	P	NA
H	CD	R	NA

NOTES (THIS DETAIL)

1. 2X Faceplate (See 2070 System PCB Module, Detail 9-7-6).

2. Connectors C2S & C20S shall be mounted on the front plate and shall be M14 AMP with Spring Latch supports or equal.

TITLE: MODEL 2070-6A, 6B ASYNC/MODEM SERIAL COMM MODULE		
	NO SCALE	
	MARCH 29, 2002	10-5-1



2070-7A (DB-9S)	
C21 & C22 CONNECTOR PINOUT	
PIN	FUNCTION
1	DCD
2	RXD
3	TXD
4	NA
5	ISO DC GND
6	NA
7	RTS
8	CTS
9	NA

2070-7B (DB-15S)			
C21 & C22 CONNECTOR PINOUT			
PIN	FUNCTION	PIN	FUNCTION
1	TX DATA +	9	TX DATA -
2	ISO DC GND	10	ISO DC GND
3	TX CLOCK +	11	TX CLOCK -
4	ISO DC GND	12	ISO DC GND
5	RX DATA +	13	RX DATA -
6	ISO DC GND	14	ISO DC GND
7	RX CLOCK +	15	RX CLOCK -
8	NA		

NOTES (THIS DETAIL)

1. 2X Faceplate (See 2070 System PCB Module, Detail 9-7-6).

2. Connectors 21 & 22 are DB 9S for Module 7A & DB 15S for Module 7B.

TITLE: MODEL 2070-7A, 7B ASYNC/SYNC SERIAL COMM MODULE	
NO SCALE	
MARCH 29, 2002	10-5-2

CHAPTER 11

2070 / NEMA STANDARD CONTROLLER UNITS

TABLE OF CONTENTS

CHAPTER 11 SECTION 1

GENERAL

11.1.1
This specification covers two versions of 2070 / NEMA Standard Controller Units. The versions associate with NEMA TS1 and NEMA TS2 Type 1 Standards. They are as follows:

Model 2070 (V or L) N1 Controller Unit (TS1)
Model 2070 (V or L) N2 Controller Unit (TS2-1)

11.1.2
The MODEL 2070 (V or L) N1 CONTROLLER UNIT consists of:

Unit CHASSIS
2070- 1A or 1B CPU Module
2070-2B Field I/O Module
2070-3B Front Panel Module
2070-4N (A or B) Power Supply Module
(2070-5 VME Cage Assembly, if required)
2070-8 Field I/O Module

11.1.3
The MODEL 2070 (V or L) N2 CONTROLLER UNIT consists of :

Unit CHASSIS
2070-1A or 1B CPU Module
2070-2N Field I/O Module
2070-3B Front Panel Module
2070-4N (A or B) Power Supply Module
(2070-5 VME Cage Assembly, if required)

11.1.4
The Serial Port 5 Frame Address for 2070-2N and 2070-8 shall be “20”.

CHAPTER 11 SECTION 2

2070-2N FIELD IO MODULE

11.2.1
The 2070-2N Field I/O Module provides a TS2-1 compatible SDLC interface via 2070 Serial Port 3, AC Power to the 2070 Unit and Fault Monitor Logic Output via 2070 Serial Port 5 and Output Frame Byte 9 Bit 6 to the NEMA TS2 Cabinet Monitor Unit (CMU).

11.2.2
The Module shall meet the 2070–2A Module Requirements with the following exceptions:

No C1, C11 and C12 Connectors on the front panel of the module
No 64 inputs / 64 outputs requirements
Serial Port 5 routed to the FCU MPU Device only
Serial Port 3 shall not have a disabling switch

11.2.3
The module shall be a 4X type board/front panel with three connectors. The connectors are 10 Pin Connector A, a NEMA 5-15 Receptacle and a 15 Pin DB 15S C14 Connector.

11.2.4
Incoming 2070 AC Power is derived from Connector A Pin C (AC+), Pin A (AC-), and Pin H (Equipment Ground). The power is directly routed to the NEMA 5-15 Receptacle. Connector A shall be a NEMA TS2 Type 1 (MS3106O-18-1S).

11.2.5
The module shall isolate 2070 Serial Port 3 from the Ax Connector and reconvert the lines to external ETA 485 drivers/receivers which shall be terminated at C14 Connector. The Port shall be clocked at 153.6 Kbps.

11.2.6
An FCU output shall drive a open collector transistor whose output shall be routed to Connector A Pin F for use as a FAULT MONITOR Output. The transistor shall be capable of sinking 200 ma at 30 VDC.

11.2.7
Connectors A and C14 pinout and functions are as follows:

CONNECTOR A

Pin	Function	Pin	Function	Pin	Function
A	AC Neutral	E	NA	I	NA

B	**NA**	**F**	**Fault Monitor**	**J**	**NA**
C	**AC Line**	**G**	**DC#2 Ground**		
D	**NA**	**H**	**Equip Ground**		

CONNECTOR C14S:

Pin	Function	Pin	Function	Pin	Function
1	**TX Data+**	**6**	**DC Ground**	**11**	**TX Clock -**
2	**DC Ground**	**7**	**RX Clock +**	**12**	**Equip Ground**
3	**TX Clock+**	**8**	**DC Ground**	**13**	**RX Data -**
4	**DC Ground**	**9**	**TX Data -**	**14**	**NA**
5	**RX Data+**	**10**	**NA**	**15**	**RX Clock –**

11.2.8

Serial Port 3 shall control the TS2 BIU Units using SDLC Protocol that meets the NEMA TS2 Type 1 Frame Command / Response Standards.

CHAPTER 11 SECTION 3

2070-4N (A or B) POWER SUPPLY MODULE

11.3.1
The 2070-4N Power Supply Module supports the NEMA TS 1 and TS2 Standards. The module is identical to the 2070-4N (A and B) Power Supply Requirements except for the following:

1) **The power cord shall have a 15 inch ± 1 inch length as measured from the panel to the plug tips.**
2) **The AC Power Fail voltage shall be 85VAC ±2VAC.**
3) **The AC Power Restore voltage shall be 90VAC ±2VAC.**
4) **The 2070-4N (A or B) power supply shall have proper marking Example "2070 4N (A or B)". A permanent sticker shall be an acceptable marking method.**

CHAPTER 11 SECTION 4

MODEL 2070- 8 FIELD I/O MODULE

11.4.1
The Module shall CONSIST OF the Module Chassis, Module Power Supply, FCU Controller, Parallel Input/Output Ports, Serial Communications Circuits and Module Connectors. The Module CHASSIS shall be made of 1.524 mm minimum aluminum sheet and treated with clear chromate. All external screws, except where called out, shall be countersunk and shall be Phillips flat head stainless steel. The matching nuts shall be permanently captive on the mating surfaces.

11.4.2
The MODULE FRONT PANEL shall be furnished with the following:

1. **ON/OFF POWER Switch mounted vertically with ON in the UP position.**
2. **LED DC Power Indicator. The indicator shall indicate that the required + 5 VDC is within 5% and the +24 VDC is within 8%.**
3. **Incoming VAC fuse protection.**
4. **Two DB-25S COMM connectors labeled "EX1" & "EX2."**
5. **Four NEMA Connectors A, B, C, & D.**

11.4.3.1
A permanent LABEL shall be affixed to the Front Panel. The label shall display the unit's serial number. The number shall be permanent and easy to read.

11.4.4
A MODULE POWER SUPPLY shall be provided and located on the right side of the module as viewed from the front. The supply shall provide the necessary module internal circuitry DC power plus 2.0 Amperes minimum of +24 VDC for external logic, detector inputs, and output load control. The supply shall meet the following requirements:

11.4.4.1
Specification 9.5.3 INPUT PROTECTION

11.4.4.2
Specification 9.5.6 POWER SUPPLY REQUIREMENTS except Spec 9.5.3.

11.4.4.3
DC Voltage tolerances shall be ±3 %.

11.4.5
The supplied INCOMING AC POWER shall be derived from Connector A Pins "p" (AC+) and "U" (AC Neutral). External +24 VDC shall be at Connector A, Pin "B" and Connector D Pin "NN." AC Power for the 2070 receptacle shall be tapped off from the secondary side of the ON Switch / Fuse configuration.

11.4.6
A MODULE PC Boards shall be mounted vertically.

11.4.7
Power Down, NRESET, and LINESYNC shall be routed to the module via C12 Connector. The state of the module output ports at the time of Power Down transition to LOW State and until NRESET goes HIGH shall be an open circuit.

11.4.8
The Module shall meet all requirements under CHAPTER 9 SECTION 3 with the following exceptions:

11.4.8.1
PARALLEL PORTS - 118 Bits of Input and 102 bits of Output shall be provided. Specification for inputs applies except the voltage is +24 in lieu of +12 and Ground False, "0," exceeds 16.0 VDC. LINESYNC signal is incoming in differential logic.

11.4.8.2
SERIAL COMMUNICATION CIRCUITRY - The module shall interface with the 2070-2B Field I/O module via HAR 1 Harness meeting EIA-485 Requirements. All signal lines shall be isolated. HAR 1 Harness shall be 17 lines minimum with a C12P Connector on one end and soldered with strain relief on the other. In addition to the Controller interface, the EIA-485 Signal lines shall be routed to EX1 Connector. All necessary driver/receiver and isolation circuitry shall be provided.

11.4.9
An EIA-232 Serial Port shall be provided with rate selection by jumper of 0.3, 1.2, 2.4, 4.8, 9.6, 19.2, & 38.4 Kbps asynchronous and shall be connected at EX1 Connector.

11.4.10
A 22-line minimum HAR 2 Harness shall be provided between EX2 Connector and Model 2070-6 Serial COMM Module in the 2070 UNIT. This provides two Modems or EIA-232 Interfaces with the 2070 UNIT and the outside world.

10.4.11
FAULT and VOLTAGE MONITOR circuitry – NEMA TS1 Controller FAULT and VOLTAGE MONITOR functions (outputs to cabinet monitor) shall be provided.

11.4.11.1
Two 3-input OR gates shall be provided. The gate 1 output shall be connected to Connector A, Pin A (FAULT MONITOR) and gate 2 output shall be connected to Connector A, Pin C. Any FALSE state input shall cause a gate output FALSE (+24VDC) state.

11.4.11.2
The FCU Port 10, Bit 7 output shall normally change its state every 100 ms. A MODULE Watchdog (WDT) circuit shall monitor the output. No state change for 2 ±0.1 seconds shall cause the circuit output to generate a FALSE (+24 VDC) output (input to gates 1 and 2).

Should the FCU begin changing state, the WDT output shall return to TRUE (0 VDC) state.

11.4.11.3
The module shall have a +5 VDC monitoring circuit which monitors the module's +5 VDC (±0.25). If the voltage exceeds the limits, the circuit output shall generate a FALSE output (input to gates 1 and 2). Normal operation shall return the output state to TRUE state.

11.4.11.4
The FCU microprocessor output shall be assigned to FAULT Monitor (input to gate 1) and another output shall be assigned to VOLTAGE Monitor (input to gate 2).

11.4.11.5
CPU Port 5 SET OUTPUT COMMAND Message OUTPUTs O78 and O79 shall be assigned to FAULT (O78) and VOLTAGE (O79). The bit logic state "1" shall be FCU output FALSE.

10.4.11.6
CPU / FCU operation at POWER UP shall be as follows:

1. **FCU Comm Loss Flag set. FAULT and VOLTAGE MONITOR outputs set to FALSE state.**
2. **CPU REQUEST MODULE STATUS COMMAND Message with "E" bit set is sent to FCU to clear Comm Loss Flag and responses to CPU with "E" bit set.**
3. **Before the Comm Loss timer expires, the SET OUTPUT COMMAND data must be sent. In that data, the 078 and 079 logically set to "0" will cause the FCU microprocessor port pins assigned for FM and VM outputs to go to their TRUE state. At this point, the signal outputs defined in the message will be permitted at the output connectors. Any number of other messages may be sent between the MODULE STATUS COMMAND and SET OUTPUTS COMMAND.**
4. *** If the above message sequence is not followed, Comm Loss Flag shall be set (or remain) and VM & FM shall retain the FALSE output state.**
5. **This is operational and preceded User Software.**

112.4.11.7
A CPU / FCU Communications Loss during normal operation shall cause all outputs to go blank (FALSE state) and shall set the Comm Loss Flag. FM and VM outputs shall be in FALSE state.

CHAPTER 11 SECTION 5

CHAPTER DETAILS

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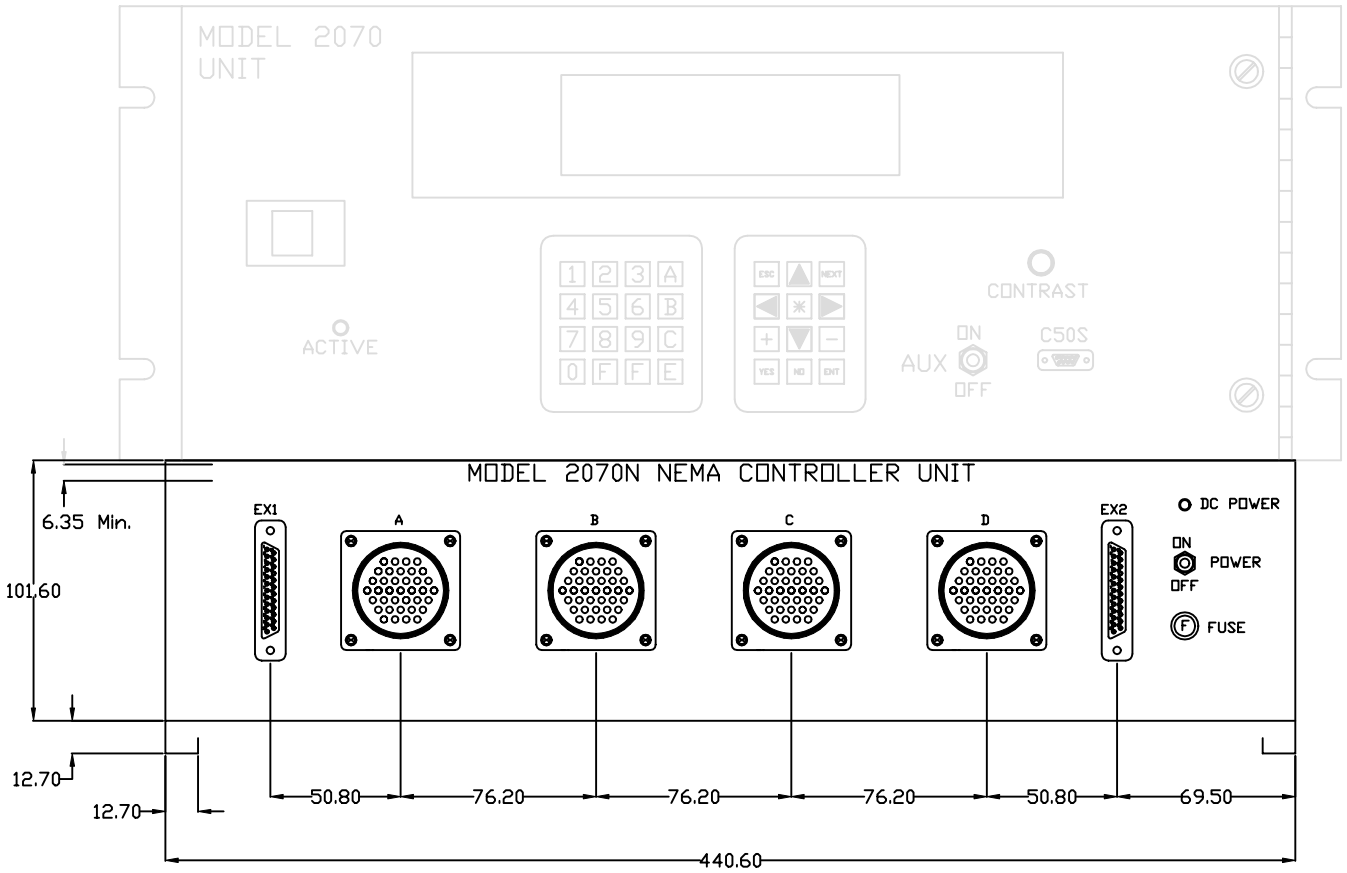
Section Notes:
All dimensions are in millimeters.
Module sheet metal tolerance shall be 0.38 mm or less.



NOTES (THIS DETAIL)

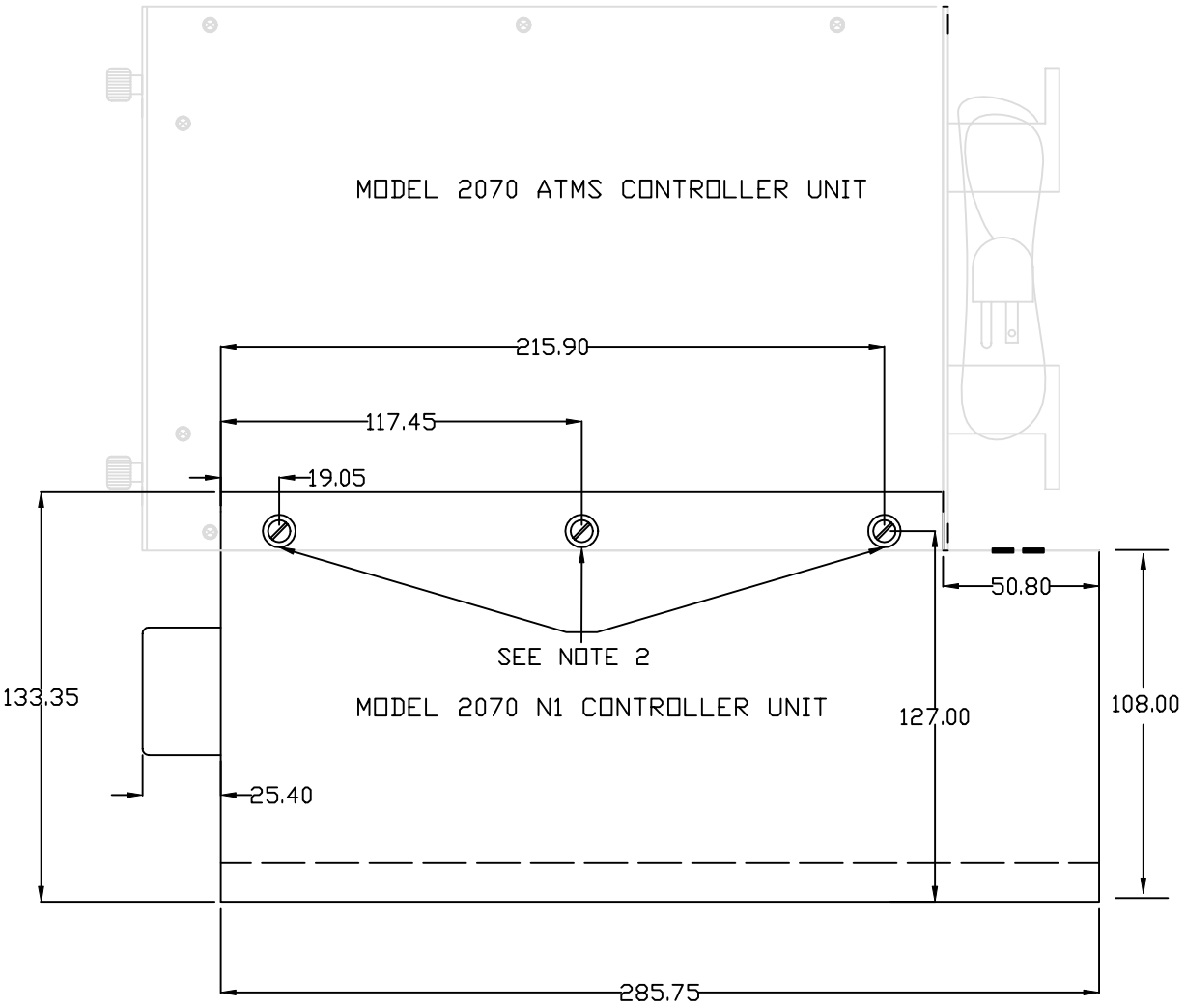
1. The Model 2070 Controller Unit is shown only for refernce.

2. The bottom supports shall be double flanged.

3. A = Connector A (MS-3112-22-55P Type)
   B = Connector B (MS-3112-22-55S Type)
   C = Connector C (MS-3112-24-61S Type)
   D = Connector D (MS-3112-24-61P Type)
   EX1 = Connector EX1 (DB-25S Type)
   EX2 = Connector EX2 (DB-25S Type)

4. 2.286 mm wide spacers shall be provided between the inside wall of the 2070-8 Module and the 2070 unit (each side).

	TITLE: 2070 (V or L) N1 CONTROLLER UNIT FRONT VIEW	
	NO SCALE	
	MARCH 29, 2002	11-5-1

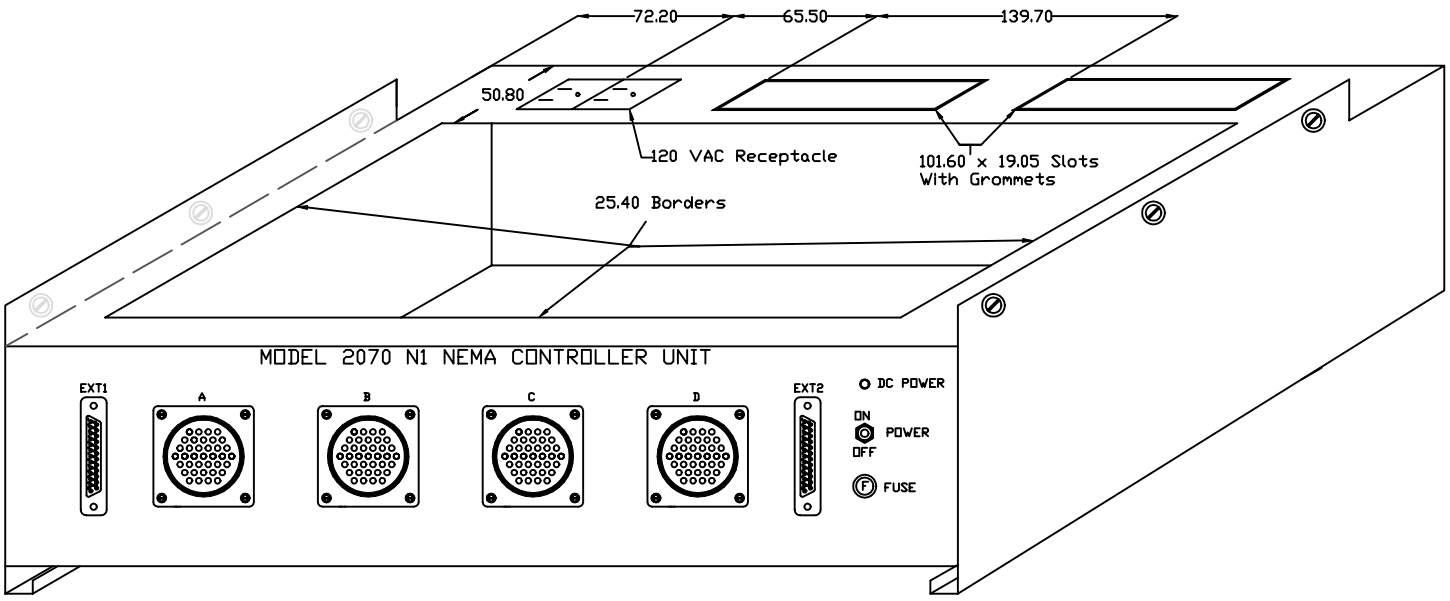


NOTES (THIS DETAIL)

1. The Model 2070 Controller Unit is shown only for reference.

2. TDS #3 Thumbscrew Devices. Module shall provide mating nuts permanently mounted on the module.

	TITLE: 2070 (V or L) N1 CONTROLLER UNIT SIDE VIEW	
	NO SCALE	
	MARCH 29, 2002	11-5-2



NOTES (THIS DETAIL)

1. The module housing bottom shall be slot vented. The top shall be open.

	TITLE: 2070 N1 CONTROLLER UNIT ISO VIEW	
	NO SCALE	
	MARCH 29, 2002	11-5-3

	CONNECTOR A			CONNECTOR B		
PIN	FUNCTION	I/O	PORT-BIT	FUNCTION	I/O	PORT-BIT
A	Fault Monitor	---	---	Phase 1 Next	Out	8-1
B	+24 VDC External	---	---	Reserved	In	9-5
C	Voltage Monitor	---	---	Phase 2 Next	Out	8-2
D	Phase 1 Red	Out	1-1	Phase 3 Green	Out	3-3
E	Phase 1 Don't Walk	Out	4-1	Phase 3 Yellow	Out	2-3
F	Phase 2 Red	Out	1-2	Phase 3 Red	Out	1-3
G	Phase 2 Don't Walk	Out	4-2	Phase 4 Red	Out	1-4
H	Phase 2 Ped Clear	Out	5-2	Phase 4 Ped Clear	Out	5-4
J	Phase 2 Walk	Out	6-2	Phase 4 Don't Walk	Out	4-4
K	Phase 2 Vehicle Detector	In	1-2	Phase 4 Check	Out	7-4
L	Phase 2 Pedestrian Detector	In	2-2	Phase 4 Vehicle Detector	In	1-4
M	Phase 2 Hold	In	3-2	Phase 4 Pedestrian Detector	In	2-4
N	Stop Timing (Ring 1)	In	6-2	Phase 3 Vehicle Detector	In	1-3
P	Inh Max Term (Ring 1)	In	6-3	Phase 3 Pedestrian Detector	In	2-3
R	External Start	In	8-1	Phase 3 Omit	In	5-3
S	Interval Advance	In	8-2	Phase 2 Omit	In	5-2
T	Indicator Lamp Control	In	8-3	Phase 5 Ped Omit	In	4-5
U	AC Neutral	---	---	Phase 1 Omit	In	5-1
V	Chassis Ground	---	---	Ped Recycle (Ring 2)	In	7-5
W	2070N DC Ground	---	---	Reserved	In	9-6
X	Flashing Logic Out	Out	11-7	Reserved	In	9-7
Y	Coded Status Bit C (Ring 1)	Out	12-3	Phase 3 Walk	Out	6-3
Z	Phase 1 Yellow	Out	2-1	Phase 3 Ped Clear	Out	5-3
a	Phase 1 Ped Clear	Out	5-1	Phase 3 Don't Walk	Out	4-3
b	Phase 2 Yellow	Out	2-2	Phase 4 Green	Out	3-4
c	Phase 2 Green	Out	3-2	Phase 4 Yellow	Out	2-4
d	Phase 2 Check	Out	7-2	Phase 4 Walk	Out	6-4
e	Phase 2 On	Out	9-2	Phase 4 On	Out	9-4
f	Phase 1 Vehicle Detector	In	1-1	Phase 4 Next	Out	8-4
g	Phase 1 Pedestrian Detector	In	2-1	Phase 4 Omit	In	5-4
h	Phase 1 Hold	In	3-1	Phase 4 Hold	In	3-4
i	Force Off (Ring 1)	In	6-1	Phase 3 Hold	In	3-3
j	Min Recall All Phases	In	8-4	Phase 3 Ped Omit	In	4-3
k	Manual Control Enable	In	8-5	Phase 6 Ped Omit	In	4-6
m	Call To Non-Actuated I	In	6-8	Phase 7 Ped Omit	In	4-7
n	Test Input A	In	9-1	Phase 8 Ped Omit	In	4-8
p	AC Power	---	---	Overlap A Yellow	Out	10-2
q	I/O Mode Bit A	In	8-6	Overlap A Red	Out	10-3
r	Coded Status Bit B (Ring 1)	Out	12-2	Phase 3 Check	Out	7-3
s	Phase 1 Green	Out	3-1	Phase 3 On	Out	9-3
t	Phase 1 Walk	Out	6-1	Phase 3 Next	Out	8-3
u	Phase 1 Check	Out	7-1	Overlap D Red	Out	11-6
v	Phase 2 Ped Omit	In	4-2	Reserved	In	9-8
w	Omit All-Red Clear (Phase 1)	In	6-7	Overlap D Green	Out	11-4
x	Red Rest Mode (Ring 1)	In	6-4	Phase 4 Ped Omit	In	4-4
y	I/O Mode Bit B	In	8-7	Not Assigned	---	---
z	Call To Non-Actuated II	In	7-8	Max II Selection (Ring 2)	In	7-6
AA	Test Input B	In	9-2	Overlap A Green	Out	10-1
BB	Walk Rest Modifier	In	9-4	Overlap B Yellow	Out	10-5
CC	Coded Status Bit A (Ring 1)	Out	12-1	Overlap B Red	Out	10-6
DD	Phase 1 On	Out	9-1	Overlap C Red	Out	11-3
EE	Phase 1 Ped Omit	In	4-1	Overlap D Yellow	Out	11-5
FF	Pedestrian Recycle (Ring 1)	In	6-5	Overlap C Green	Out	11-1
GG	Max II Selection (Ring 1)	In	6-6	Overlap B Green	Out	10-4
HH	I/O Mode Bit C	In	8-8	Overlap C Yellow	Out	11-2

TITLE:

2070-8 FIELD I/O MODULE CONNECTORS A & B

NO SCALE

MARCH 29, 2002

	CONNECTOR C			CONNECTOR D		
PIN	FUNCTION	I/O	PORT-BIT	FUNCTION	I/O	PORT-BIT
A	Coded Status Bit A (Ring 2)	Out	12-4	Detector 9	In	10-1
B	Coded Status Bit B (Ring 2)	Out	12-5	Detector 10	In	10-2
C	Phase 8 Don't Walk	Out	4-8	Detector 11	In	10-3
D	Phase 8 Red	Out	1-8	Detector 12	In	10-4
E	Phase 7 Yellow	Out	2-7	Detector 13	In	10-5
F	Phase 7 Red	Out	1-7	Detector 14	In	10-6
G	Phase 6 Red	Out	1-6	Detector 15	In	10-7
H	Phase 5 Red	Out	1-5	Detector 16	In	10-8
J	Phase 5 Yellow	Out	2-5	Detector 17	In	11-1
K	Phase 5 Ped Clear	Out	5-5	Detector 18	In	11-2
L	Phase 5 Don't Walk	Out	4-5	Detector 19	In	11-3
M	Phase 5 Next	Out	8-5	Detector 20	In	11-4
N	Phase 5 On	Out	9-5	Detector 21	In	11-5
P	Phase 5 Vehicle Detector	In	1-5	Detector 22	In	11-6
R	Phase 5 Pedestrian Detector	In	2-5	Detector 23	In	11-7
S	Phase 6 Vehicle Detector	In	1-6	Detector 24	In	11-8
T	Phase 6 Pedestrian Detector	In	2-6	Clock Update	In	12-1
U	Phase 7 Pedestrian Detector	In	2-7	Hardware Control	In	12-2
V	Phase 7 Vehicle Detector	In	1-7	Cycle Advance	In	12-3
W	Phase 8 Pedestrian Detector	In	2-8	Max 3 Selection	In	12-4
X	Phase 8 Hold	In	3-8	Max 4 Selection	In	12-5
Y	Force Off (Ring 2)	In	7-1	Free	In	12-6
Z	Stop Timing (Ring 2)	In	7-2	Not Assigned	In	12-7
a	Inhibit Max Timing (Ring 2)	In	7-3	Not Assigned	In	12-8
b	Test Input C	In	9-3	Alarm 1	In	13-1
c	Coded Status Bit C (Ring 2)	Out	12-6	Alarm 2	In	13-2
d	Phase 8 Walk	Out	6-8	Alarm 3	In	13-3
e	Phase 8 Yellow	Out	2-8	Alarm 4	In	13-4
f	Phase 7 Green	Out	3-7	Alarm 5	In	13-5
g	Phase 6 Green	Out	3-6	Flash In	In	13-6
h	Phase 6 Yellow	Out	2-6	Conflict Monitor Status	In	13-7
i	Phase 5 Green	Out	3-5	Door Ajar	In	13-8
j	Phase 5 Walk	Out	6-5	Special Function 1	In	14-1
k	Phase 5 Check	Out	7-5	Special Function 2	In	14-2
m	Phase 5 Hold	In	3-5	Special Function 3	In	14-3
n	Phase 5 Omit	In	5-5	Special Function 4	In	14-4
p	Phase 6 Hold	In	3-6	Special Function 5	In	14-5
q	Phase 6 Omit	In	5-6	Special Function 6	In	14-6
r	Phase 7 Omit	In	5-7	Special Function 7	In	14-7
s	Phase 8 Omit	In	5-8	Special Function 8	In	14-8
t	Phase 8 Vehicle Detector	In	1-8	Preempt 1 In	In	15-1
u	Red Rest Mode (Ring 2)	In	7-4	Preempt 2 In	In	15-2
v	Omit All Red (Ring 2)	In	7-7	Preempt 3 In	In	15-3
w	Phase 8 Ped Clear	Out	5-8	Preempt 4 In	In	15-4
x	Phase 8 Green	Out	3-8	Preempt 5 In	In	15-5
y	Phase 7 Don't Walk	Out	4-7	Preempt 6 In	In	15-6
z	Phase 6 Don't Walk	Out	4-6	Alarm 1 Out	Out	12-7
AA	Phase 6 Ped Clear	Out	5-6	Alarm 2 Out	Out	12-8
BB	Phase 6 Check	Out	7-6	Special Function 1 Out	Out	13-1
CC	Phase 6 On	Out	9-6	Special Function 2 Out	Out	13-2
DD	Phase 6 Next	Out	8-6	Special Function 3 Out	Out	13-3
EE	Phase 7 Hold	In	3-7	Special Function 4 Out	Out	13-4
FF	Phase 8 Check	Out	7-8	Special Function 5 Out	Out	13-5
GG	Phase 8 On	Out	9-8	Special Function 6 Out	Out	13-6
HH	Phase 8 Next	Out	8-8	Special Function 7 Out	Out	13-7
JJ	Phase 7 Walk	Out	6-7	Special Function 8 Out	Out	13-8
KK	Phase 7 Ped Clear	Out	5-7	Not Assigned	---	---
LL	Phase 6 Walk	Out	6-6	Detector Reset	Out	11-8
MM	Phase 7 Check	Out	7-7	Not Assigned	---	---
NN	Phase 7 On	Out	9-7	+24 VDC	---	---
PP	Phase 7 Next	Out	8-7	2070N DC Gnd	---	---

TITLE:
2070-8 FIELD I/O MODULE CONNECTORS C & D

NO SCALE

MARCH 29, 2002

11-5-5

EX1 CONNECTOR PINOUT	
PIN	FUNCTION
1	EQ GND
2	TXD FCU
3	RXD FCU
4	RTS FCU
5	CTS FCU
6	NA
7	2070-8 DC GND
8	DCD FCU
9	2070-8 DC GND
10	485 TX Data+
11	485 TX Data-
12	485 TX Clock+
13	485 TX Clock-
14	2070-8 DC GND
15	485 RX Data+
16	485 RX Data-
17	2070-8 DC GND
18	485 RX Clock+
19	485 RX Clock-
20	NA
21	NA
22	NA
23	NA
24	NA
25	NA

EX2 CONNECTOR PINOUT	
PIN	FUNCTION
1	EQ GND
2	TXD 1
3	RXD 1
4	RTS 1
5	CTS 1
6	NA
7	DC GND #1
8	DCD 1
9	AUDIO IN 1
10	AUDIO IN 1
11	AUDIO OUT 1
12	AUDIO OUT 1
13	NA
14	EQ GND
15	TXD 2
16	RXD 2
17	RTS 2
18	CTS 2
19	NA
20	DC GND #1
21	DCD 2
22	AUDIO IN 2
23	AUDIO IN 2
24	AUDIO OUT 2
25	AUDIO OUT 2

TITLE:

2070-8 FIELD I/O MODULE EX1 & EX2 CONNECTOR

	NO SCALE	
	MARCH 29, 2002	11-5-6